MACH™ 3 and 4 Family Data Book

2nd Generation High Density EE CMOS Programmable Logic

1993

Advanced Micro Devices

ARROW ELECTRONICS, INC.
ARROW ELECTRONICS CANADA LTD.
1093 MEYERSIDE DRIVE, UNIT 2
MISSISSAUGA, ONTARIO L5T 1M4
(416) 670-7769 FAX: (416) 670-7781

VALERIE JONES

MACH 3 and 4 Device Families

Data Book

January 1993

ADVANCED MICRO DEVICES

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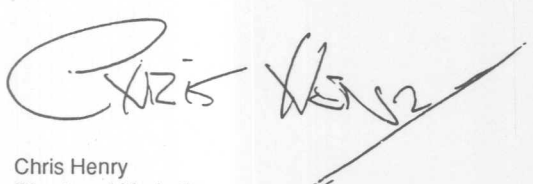
First introduced in Fall 1990, MACH™ (Macro Array CMOS High-density) devices have set the industry standard for 15-nanosecond predictable worst-case pin-to-pin delays for devices ranging from 900 to 3600 gates. For the first time, higher-density EE CMOS PAL®-like devices with truly predictable speeds were widely available. FPGA and high-density customers responded enthusiastically, resulting in thousands of designs wins and over one million MACH devices shipped.

Based on your feedback, we are introducing the second generation of MACH devices – the MACH 3 and 4 device family. Like the first generation MACH 1 and 2 devices, these new MACH devices have been the same, truly predictable pin-to-pin delays, but offer greater densities, increased flexibility, and higher-pin count packages. MACH 3 and 4 family devices feature synchronous or asynchronous operation, gate densities from 3700 to 10,000 gates, and 84 to 196 pins in PLCC and PQFP packages.

In just a few short years, AMD has become a major force in CMOS PLDs, building on our #1 spot in bipolar to become the industry leader in CMOS as well. Given the benefits of our advanced 0.65 micron double metal EE CMOS technology, we promise to continue providing the fastest and most innovative programmable logic devices, making it ever easier to get new products to market quickly.



Chris Henry
Director of Marketing
Programmable Logic

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MACH 3 and 4 Device Families

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High-performance, high-density electrically-erasable CMOS PLD families**
- **Predictable design-independent 15- and 20-ns speeds**
- **High density, pin count**
  - — 3700–10,000 gate equivalents
  - — 84–196 pins
  - — 96–384 registers
- **Input and output switch matrices increase ability to hold a fixed pinout**
- **JTAG, 5-V in-circuit programmability on devices with more than 84 pins**
- **Synchronous and asynchronous modes available for each macrocell**
  - — clock generator in each PAL® block for programmable clocks, edges in either mode
  - — individual clock, initialization product terms in asynchronous mode
- **Central, input, and output switch matrices**
  - — 100% routability with 80% utilization
- **Up to 20 product terms per function**
- **96–256 configurable macrocells**
  - — D/T/J-K/S-R registers, latches
  - — synchronous or asynchronous mode
  - — programmable polarity
  - — reset/preset swapping
- **XOR gate available**
- **Registered/latched inputs on MACH 4 series**
- **Extensive third-party software and programmer support through FusionPLD℠ partners**

PRODUCT SELECTOR GUIDE

Device	Pins	Macrocells	Gate Equiv	Max Inputs	Max Outputs	Max Flip-Flops	JTAG/ 5 V Prog	Speed
MACH 3 Family								
MACH355	132	96	3500	102	96	96	Y	15, 20
MACH 4 Family								
MACH435	84	128	5000	70	64	192	N	15, 20
MACH445	100	128	5000	70	64	192	Y	15, 20
MACH465	196	256	10,000	146	128	384	Y	15, 20

GENERAL DESCRIPTION

The MACH (Macro Array CMOS High-speed/density) family provides a new way to implement large logic designs in a programmable logic device. AMD has combined an innovative architecture with advanced electrically-erasable CMOS technology to offer a device with many times the logic capability of the industry's most popular existing PAL device solutions at comparable speed and cost.

The second-generation MACH devices provide approximately three times the density and register count, and two times the amount of I/O of the original MACH 1 and 2 families. By increasing the pin count, adding functionality, and improving routing, the MACH 3 and 4 families build upon the strength of the MACH architecture without sacrificing predictable timing.

Their unique architecture makes these devices ideal for replacing large amounts of TTL, PAL-device, glue, and gate-array logic. They are the first devices to provide such increased functionality with completely predictable, deterministic speed.

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Issue Date: December 1992

The MACH devices consist of PAL blocks interconnected by a programmable central switch matrix (Figure 1). Designs that consist of several interconnected functional modules can be efficiently implemented by placing the modules into PAL blocks. Designs that are not as modular can also be readily implemented since the central switch matrix provides a very high level of connectivity between PAL blocks.

The use of input and output switch matrices allows logic to be implemented independent of pin connections. This allows greater flexibility when making initial pin assignments for PCB layout, or when trying to maintain the pinout through design changes. The internal arrangement of resources is managed automatically by the design software, so that the designer does not have to be concerned with the logic implementation details.

AMD's FusionPLD program allows MACH device designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide timely, accurate, quality support. This ensures that a designer does not have to buy a complete new set of tools for each new device, but rather can use the tools with which he or she is already familiar. The MACH devices can programmed on conventional PAL device programmers. Devices with pin counts greater than 84 have an additional 5-V programming algorithm option that can be implemented with the devices soldered onto the board.

MACH devices are manufactured using AMD's state-of-the-art advanced CMOS electrically-erasable process for high performance and logic density. CMOS EE technology provides 100% testability, reducing both prototype development costs and production costs.

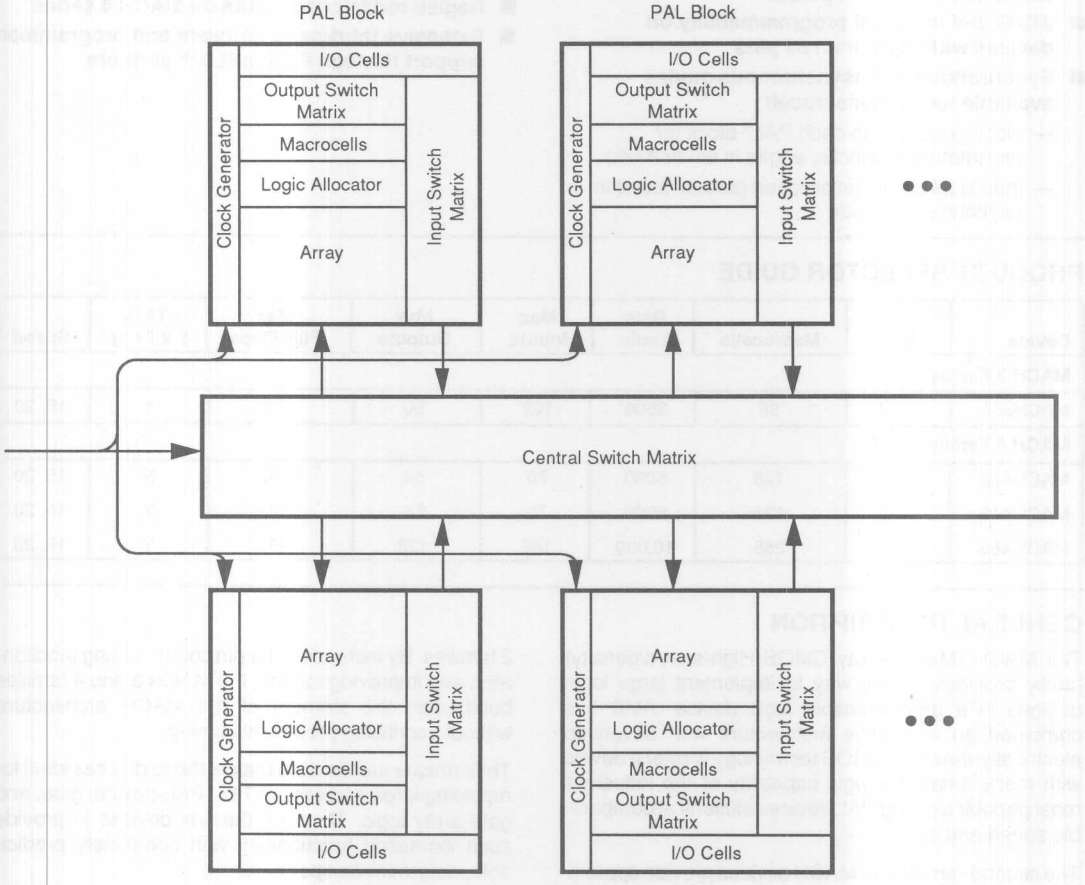

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Figure 1. MACH 3 and 4 Block Diagram

Design Methodology

Design tools for all MACH devices are widely available both from AMD and from third-party software vendors. AMD provides MACHXL™ software as a low-cost baseline tool set and works with third-party vendors to ensure broad MACH device support. MACHXL software is based on the popular PALASM® software package, with support dedicated to the higher-density MACH 3 and 4 devices. PAL devices, MACH 1 devices, and MACH 2 devices are supported by PALASM 4 software; MACH 3 and 4 devices are supported by MACHXL software. This allows designers to do MACH device designs using the same methodology that they would use to do any PLD or FPGA designs, whether with MACHXL software or any of the other popular PAL device or FPGA design packages.

Design entry can be the same as that used for PAL, MACH 1, and MACH 2 devices. The basic logic processing steps are the same steps that are needed to process and minimize logic for any PAL device. Simulation is available for verifying the correct behavior of the device. Functional (unit-delay) simulation of MACH devices is supported in all approved software packages, and other options for simulating the timing and board-level behavior of the MACH devices are available. The end result is a JEDEC file that can be downloaded to a programmer for device configuration.

MACH device design methodology differs somewhat from that of a PAL device due to the automatic design fitting procedure that the software performs. Designs written by logic designers—whether by schematic capture, state machine equations, Boolean equations, or behavioral languages—are partitioned and placed into the PAL blocks of the MACH device. While this procedure is handled automatically by the software, the software can also accept manual direction based upon the user's working knowledge of the design. The overall device utilization provided by the fitter will vary from design to design, but in general significantly higher utilization can be expected from the MACH 3 and 4 families than from the MACH 1 and 2 devices due to the additional routing resources. In addition, MACH 3 and 4 device designs with higher utilization are more likely to retain the same pinout when design changes are made since the output switch matrix allows a pin to be driven by any of a number of macrocells.

AMD recommends allowing the software to decide the best fit and pin placement automatically for the first design iteration. This will provide the best chance of fitting. With this approach, large designs can be implemented incrementally, starting with low device utilization and building up by adding logic until the device is full. This generally means that designs are done without any specific pinout assignments, with the final pinout decided by the software. It is possible to "pre-place" signals, and, given the plentiful routing resources, pre-placement is very likely to be successful on the MACH 3 and 4 families. However, the most successful design fit can still be achieved by allowing the software as much fitting flexibility as possible.

The design is partitioned and placed into the MACH device by the software so as not to affect the performance of the design. With designs that do not fit it is possible to make some performance tradeoffs to aid in fitting (for example, by optimizing the flip-flop type or passing through the device more than once), but those tradeoffs must be specifically requested, and any additional delays are entirely predictable.

Once an initial design fits, there may be subsequent changes to the design. This is important if board layout has already started based on the original pinout. A major role of the input and output switch matrices is to allow such changes without impacting the original pinout. Certain design changes may make it impossible to maintain the original pinout, but designs can easily target 80% utilization without seriously jeopardizing the ability to make design changes and maintain pinout.

SECOND GENERATION MACH DEVICES

The MACH 3 and MACH 4 families consist of several members differentiated primarily by pin count and number of macrocells. The MACH 3 family has one macrocell per I/O pin; the MACH 4 family has two macrocells per I/O pin. In addition, the MACH 4 family has input registers. The MACH 4 register count is therefore three times the I/O pin count.

The devices range in pin count from 84 to 196; in number of macrocells from 96 to 256; and in number of registers from 96 to 384. All devices above 84 pins are provided in space-saving PQFP packages, with JTAG and 5-V in-circuit programmability. The 84-pin MACH435 comes in a PLCC package, without JTAG or 5-V programming, for pin-compatibility with the MACH130 and MACH230. Its architecture is available with JTAG and 5-V programmability in the 100-pin MACH445.

Functional Description

The fundamental architecture of the MACH devices consists of multiple optimized PAL blocks interconnected by a central switch matrix. The central switch matrix allows communication between PAL blocks, and routes inputs to the PAL blocks. Together, the PAL blocks and central switch matrix allow the logic designer to create large designs in a single device instead of multiple devices.

Most pins are I/O pins that can be used as inputs, output, or bidirectional pins. There are some dedicated input pins, but all macrocells have internal feedback, allowing the pin to be used as an input if the macrocell signal is not needed externally.

The key to being able to make effective use of these devices lies in the interconnect schemes. Because of the programmable interconnections, the product term arrays have been decoupled from the central switch matrix; the macrocells have been decoupled from the product terms through the logic allocator; and the I/O pins have been decoupled from the macrocells due to the output switch matrix. In addition, more input routing options are provided by the input switch matrix. These resources provide the flexibility needed to place and route designs efficiently.

In a MACH device, all signals incur the same delays, regardless of routing. Performance is design-independent, and is known before the design is begun.

The PAL Blocks

The PAL blocks resemble independent PAL devices on the chip. This provides for logic functions that need the complete interconnect that a PAL device provides. PAL blocks communicate with each other through the central switch matrix.

Each PAL block consists of:

- a product-term array
- a logic allocator
- macrocells
- an output switch matrix
- I/O cells
- an input switch matrix
- a clock generator

The logic allocator distributes the product terms to the macrocells, as required by each individual design. The macrocell configures the signal largely by determining the storage characteristics. Macrocell signals are routed to I/O cells and the I/O pins by the output switch matrix. The I/O cells on MACH 4 devices also allow for registered or latched inputs. The input switch matrix optimizes the routing of input signals into the central switch matrix.

The clock generator uses the four global clock inputs to generate a set of four clock signals available throughout the PAL block. Various combinations of clock signals in both true and complement form can be generated.

Each PAL block also contains an asynchronous reset product term and an asynchronous preset product term to be used for synchronous-mode macrocells. This allows synchronous flip-flops within a single PAL block to be initialized as a bank. Macrocells implemented in asynchronous mode are not affected by the PAL-block initialization.

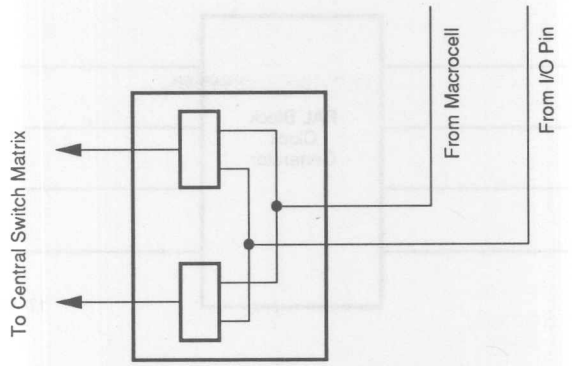
The Central Switch Matrix

The central switch matrix takes all dedicated inputs and signals from the input switch matrices and routes them as needed to the PAL blocks. Feedback signals that only return to the same PAL block still must go through the central switch matrix. This mechanism ensures that PAL blocks in MACH devices communicate with each other with consistent, predictable delays.

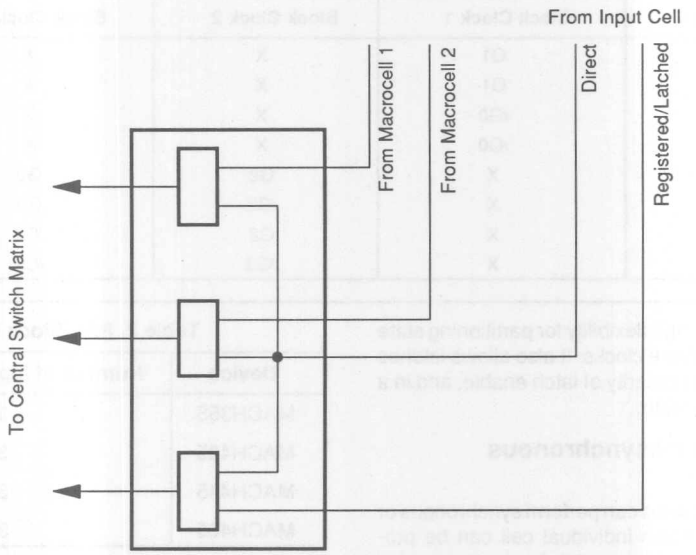
The central switch matrix makes a MACH device more than just several PAL devices on a single chip. It allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into PAL blocks through the central switch matrix so that the designer does not have to be concerned with the internal architecture of the device.

The Input Switch Matrix

The input switch matrix (Figure 2) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.



a. MACH 3; one per macrocell



b. MACH 4; one for every two macrocells

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Figure 2. Input Switch Matrix

PAL Block Clock Generation

Each MACH 3 and 4 device has four clock pins that can also be used as inputs. These pins drive a clock generator in each PAL block (Figure 3). The clock generator provides four clock signals that can be used anywhere in the PAL block. These four PAL block clock signals can consist of a large number of combinations of the true and complement edges of the global clock signals; Table 1 lists the possible combinations.

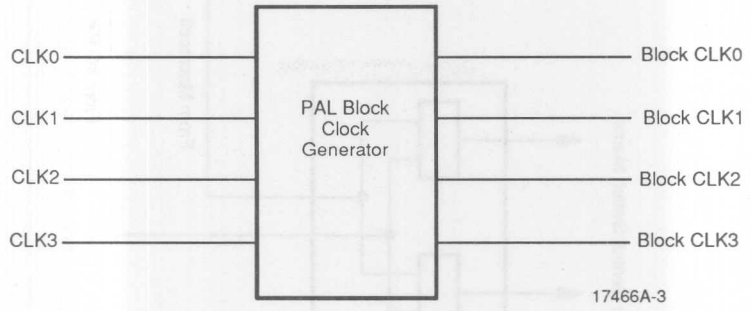


Figure 3. PAL Block Clock Generator

Table 1. PAL Block Clock Combinations

Block Clock 0	Block Clock 1	Block Clock 2	Block Clock 3
G0	G1	X	X
/G1	G1	X	X
G0	/G0	X	X
/G1	/G0	X	X
X	X	G2	G3
X	X	/G3	G3
X	X	G2	/G2
X	X	/G3	/G2

This feature provides high flexibility for partitioning state machines and dual-phase clocks. It also allows latches to be driven with either polarity of latch enable, and in a master-slave configuration.

Synchronous and Asynchronous Operation

The MACH 3 and 4 families can perform synchronous or asynchronous logic. Each individual cell can be programmed as synchronous or asynchronous, allowing unlimited "mixing and matching" of the two logic styles. The selection of synchronous or asynchronous mode affects the logic allocator and the macrocell, since product terms used for logic in the synchronous mode are used for control functions in the asynchronous mode.

The Product Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the central switch matrix (Table 2), and are provided in both true and complement forms for efficient logic implementation.

Table 2. PAL Block Inputs

Device	Number of Inputs to PAL Block
MACH355	33
MACH435	33
MACH445	33
MACH465	34

Because the number of product terms available for a given logic function is not fixed, the full sum of products is not realized in the array. The product terms drive the logic allocator, which allocates the appropriate number of product terms to generate the function.

The Logic Allocator

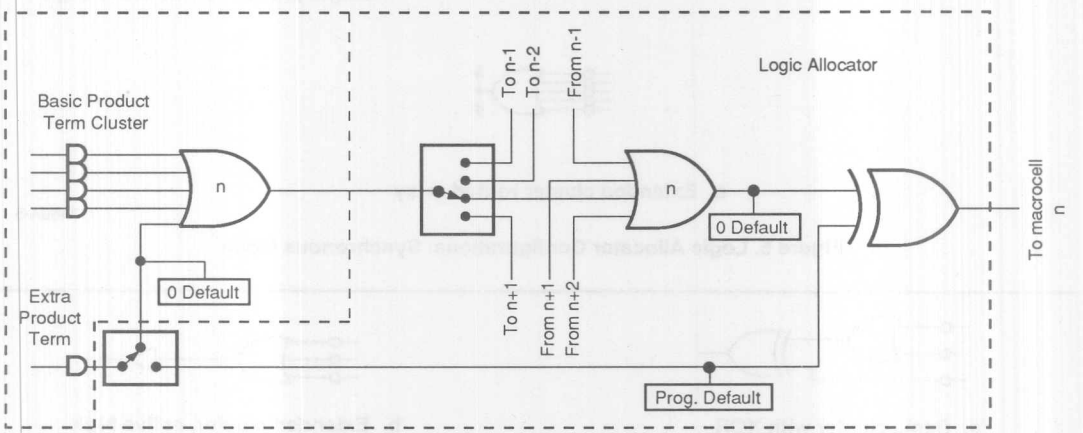
Within the logic allocator, product terms are allocated to macrocells in "product term clusters." The availability and distribution of product term clusters are automatically considered by the software as it places and routes functions within a PAL block. The size of a product term cluster has been optimized to provide high utilization of product terms, making complex functions using many

product terms possible. Yet when few product terms used, there will be a minimal number of unused—or wasted—product terms left over.

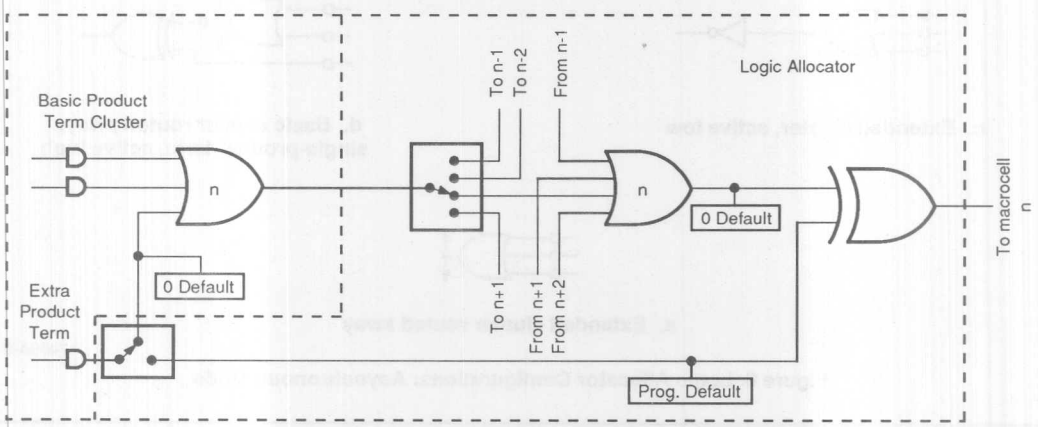
The logic allocator has two fundamental modes, depending on whether the macrocell is synchronous or asynchronous. The synchronous mode (Figure 4a) has a basic product term cluster of four product terms; the asynchronous mode (Figure 4b) has a basic cluster of two product terms. Note that if the product term cluster is routed to a different macrocell, the allocator configuration is not determined by the mode of the macrocell actually being driven. The configuration is always set by the mode of the macrocell that the cluster will drive if not routed away, regardless of the actual routing.

In addition, there is an extra product term that can either join the basic cluster to give an extended cluster, or drive the second input of an exclusive-OR gate in the signal path. If included with the basic cluster, this provides for up to 20 product terms on a synchronous function that uses four extended 5-product-term clusters. A similar asynchronous function can have up to 18 product terms.

When the extra product term is used to extend the cluster, the value of the second XOR input can be programmed as a 0 or a 1, giving polarity control. The possible configurations of the logic allocator are shown in Figures 5 and 6.



a. Synchronous Mode



b. Asynchronous Mode

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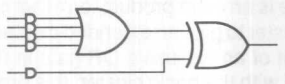
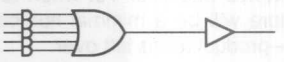
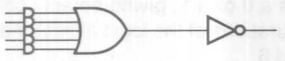
Figure 4. Logic Allocator. Configuration of cluster "n" set by mode of macrocell "n".



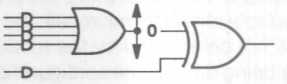
a. Basic cluster with XOR



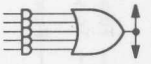
b. Extended cluster, active high



c. Extended cluster, active low



d. Basic cluster routed away; single-product-term, active high



e. Extended cluster routed away

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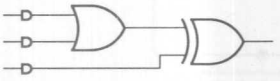
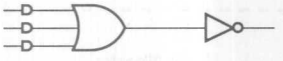
Figure 5. Logic Allocator Configurations: Synchronous Mode

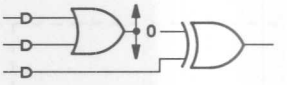


a. Basic cluster with XOR

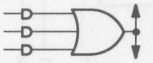
b. Extended cluster, active high



c. Extended cluster, active low



d. Basic cluster routed away; single-product-term, active high



e. Extended cluster routed away

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Figure 6. Logic Allocator Configurations: Asynchronous Mode

Note that the configuration of the logic allocator has absolutely no impact on the speed of the signal. All configurations have the same delay. This means that designers do not have to decide between optimizing resources or speed; both can be optimized.

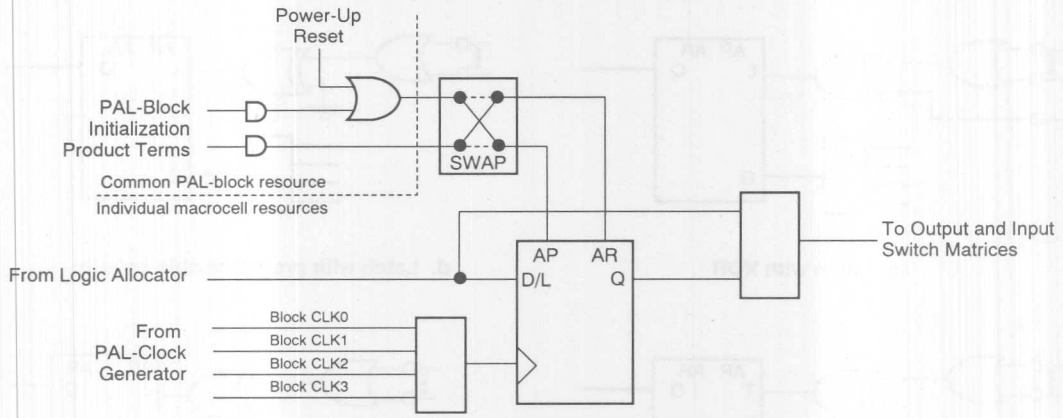
If not used in the cluster, the extra product term can act in conjunction with the basic cluster to provide XOR logic for such functions as data comparison, or it can work with the D-type flip-flop to provide for T, J-K, and S-R register operation. In addition, if the basic cluster is

routed to another macrocell, the extra product term is still available for logic. In this case, the first XOR input will be a logic 0. This circuit has the flexibility to route product terms elsewhere without giving up the use of the macrocell.

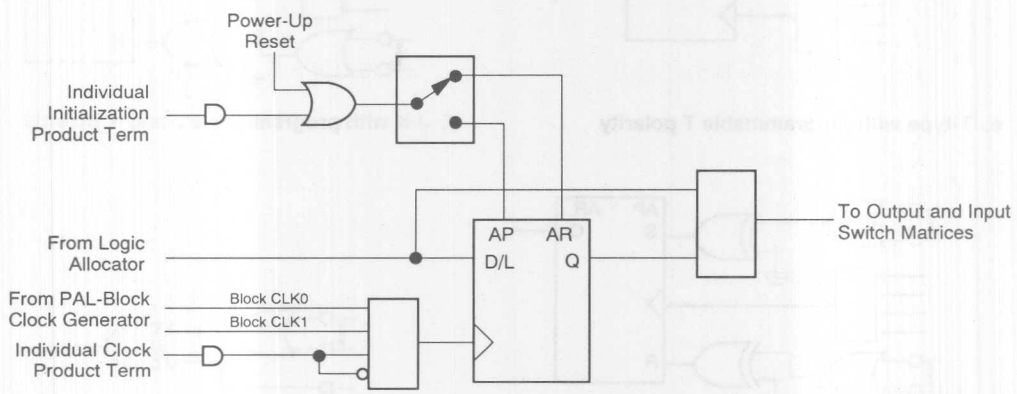
Product term clusters do not "wrap" around a PAL block. This means that the macrocells at the ends of the block have fewer product terms available. Refer to the individual product data sheets for details.

The Macrocell

The macrocell consists of a storage element, routing resources, a clock multiplexer, and initialization control. The macrocell has two fundamental modes: synchronous and asynchronous (Figure 7). The mode chosen only affects clocking and initialization in the macrocell.



a. Synchronous Mode



b. Asynchronous Mode

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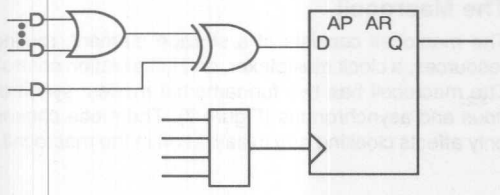
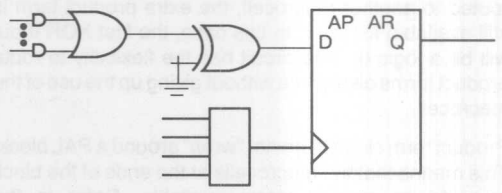
Figure 7. Macrocell

In either mode, a combinatorial path can be used. For combinatorial logic, the synchronous mode will generally be used, since it provides more product terms in the allocator.

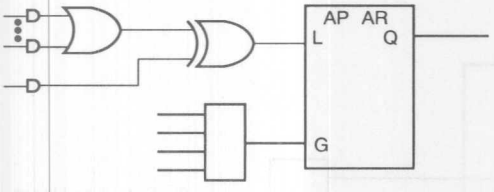
The flip-flop can be configured as a D-type, T-type, J-K, or S-R register or latch. The primary flip-flop configurations are shown in Figure 8, although others are possible. Flip-flop functionality is defined in Table 3. Note that a J-K latch is unadvisable, as it will cause oscillation if both J and K inputs are HIGH.



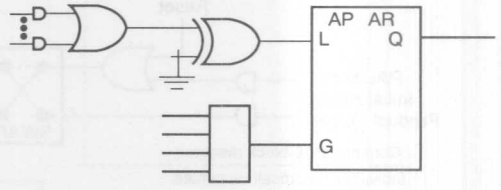
a. D-type with XOR



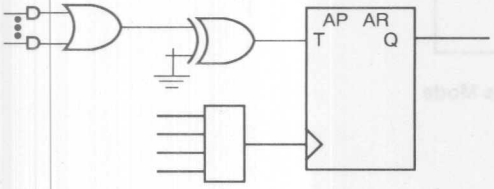
b. D-type with programmable D polarity



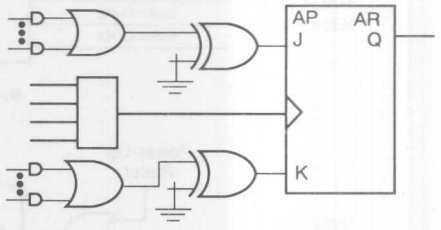
c. Latch with XOR



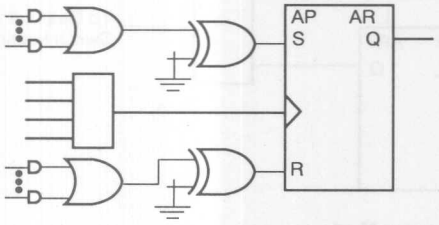
d. Latch with programmable polarity



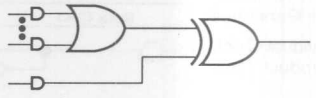
e. T-type with programmable T polarity



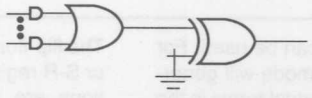
f. J-K with programmable J and K polarity



g. S-R with programmable S and R polarity



h. Combinatorial with XOR



i. Combinatorial with programmable polarity

17466A-8

Figure 8. Primary Macrocell Configurations

Table 3. Register/Latch Operation

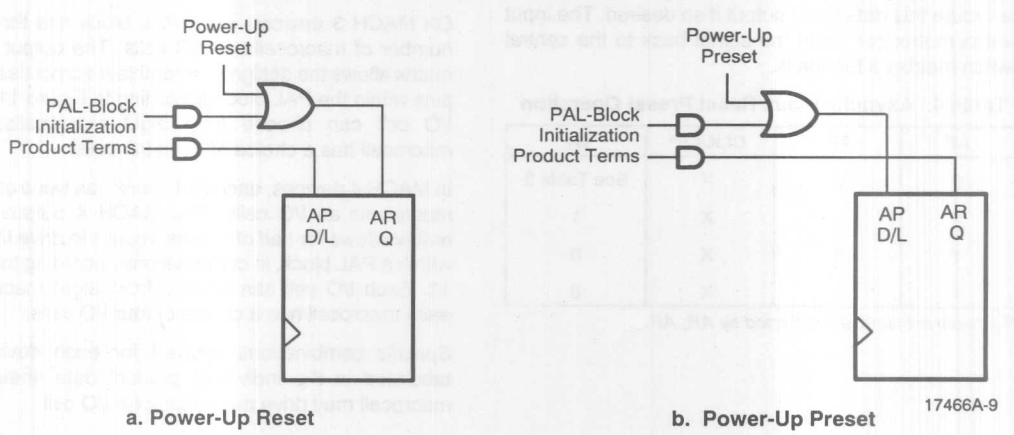
Configuration	Input(s)	CLK/LE*	Q+
D-type Register	D=X	0, 1, ↓ (↑)	Q
	D=0	↑ (↓)	0
	D=1	↑ (↓)	1
T-type Register	T=X	0, 1, ↓ (↑)	Q
	T=0	↑ (↓)	Q
	T=1	↑ (↓)	$\overline{Q}$
J-K Register	J=K=X	0, 1, ↓ (↑)	Q
	J=0, K=0	↑ (↓)	Q
	J=0, K=1	↑ (↓)	0
	J=1, K=0	↑ (↓)	1
	J=1, K=1	↑ (↓)	$\overline{Q}$
S-R Register	S=R=X	0, 1, ↓ (↑)	Q
	S=0, R=0	↑ (↓)	Q
	S=0, R=1	↑ (↓)	0
	S=1, R=0	↑ (↓)	1
	S=1, R=1	↑ (↓)	Undefined
D-type Latch	D=X	1 (0)	Q
	D=0	0 (1)	0
	D=1	0 (1)	1

**Polarity of CLK/LE can be programmed.*

Although the macrocell shows only one input to the register, the XOR gate in the logic allocator allows the D-type register to emulate T, J-K, and S-R behavior. In this case, the available product terms are divided between J and K (or S and R). When configured as J-K, S-R, or T-type, the extra product term must be used on the XOR gate input for flip-flop emulation. In any register type, the polarity of the inputs can be programmed.

The clock input to the flip-flop can select any of the four PAL block clocks in synchronous mode, with the additional choice of either polarity of an individual product term clock in the asynchronous mode.

The initialization circuit depends on the mode. In synchronous mode (Figure 9), asynchronous reset and preset are provided, each driven by a product term common to the entire PAL block.



a. Power-Up Reset

b. Power-Up Preset

Figure 9. Synchronous Mode Initialization Configurations

A subtle difference between MACH 1 and 2 devices and the MACH 3 and 4 devices is that the original devices have programmable output polarity; that is, the polarity control comes after the flip-flop. In the new MACH 3 and 4 architecture, the flip-flop input polarity is programmable. For designs that can be implemented on both the older and newer devices, this makes no difference except that in the older architecture, reset and preset values are affected by polarity; in the new architecture they are not. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility and design compatibility between the old and new architectures.

In asynchronous mode (Figure 10), a single individual product term is provided for initialization. It can be selected to control reset or preset.

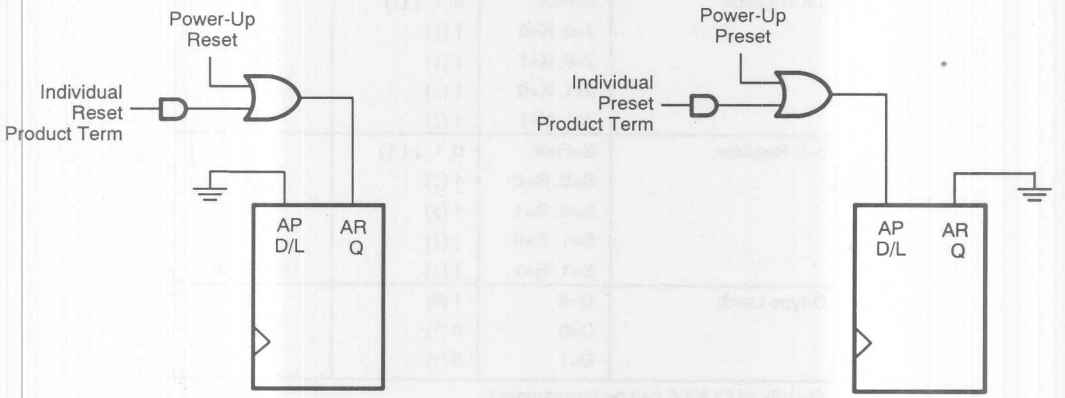


Figure 10. Asynchronous Mode Initialization Configurations

Note that the reset/preset swapping/selection feature affects power-up reset as well. The initialization functionality of the flip-flops is illustrated in Table 4.

The macrocell sends its data to the output switch matrix and the input switch matrix. The output switch matrix can route this data to an output if so desired. The input switch matrix can send the signal back to the central switch matrix as feedback.

Table 4. Asynchronous Reset/Preset Operation

AR	AP	CLK/LE*	Q+
0	0	X	See Table 3
0	1	X	1
1	0	X	0
1	1	X	0

**Transparent latch is unaffected by AR, AP.*

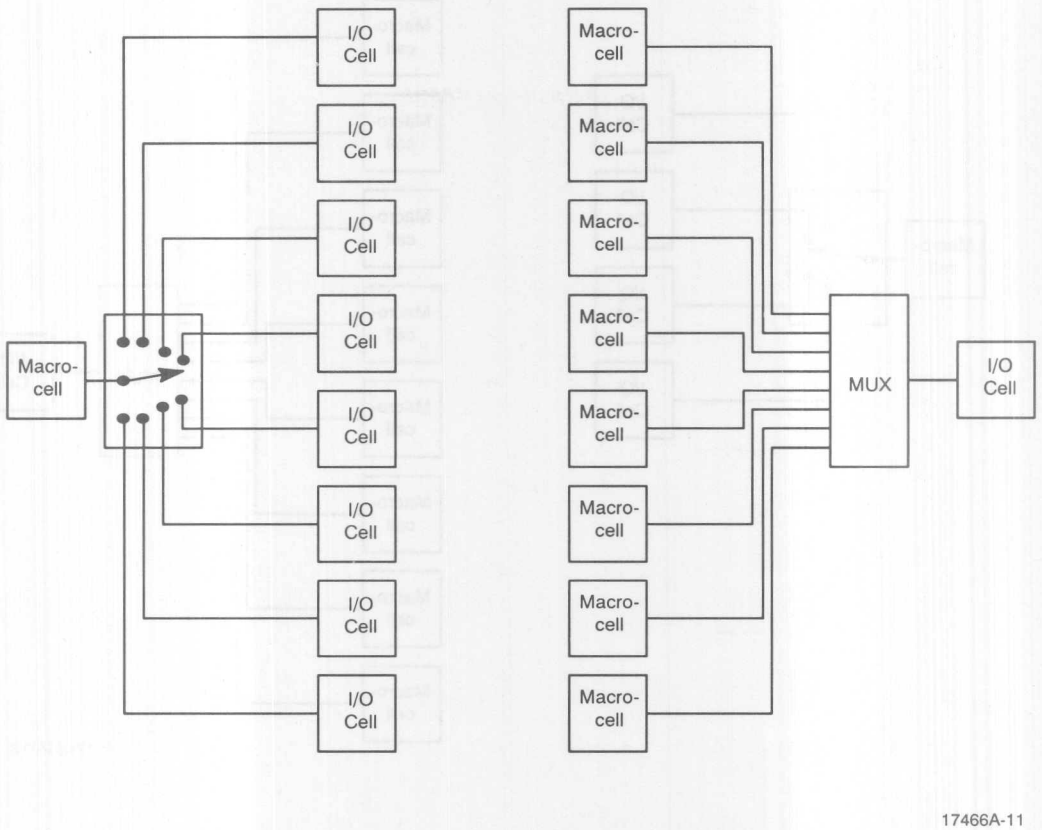
The Output Switch Matrix

The output switch matrix allows macrocells to be connected to any of several I/O cells within a PAL block. This provides high flexibility in determining pinout, and allows design changes that will not affect pinout.

On MACH 3 devices, each PAL block has the same number of macrocells as I/O cells. The output switch matrix allows the design to scramble macrocells and I/O pins within the PAL block according to Figure 11. Each I/O cell can choose from eight macrocells; each macrocell has a choice of eight I/O cells.

In MACH 4 devices, each PAL block has twice as many macrocells as I/O cells. The MACH 4 output switch matrix allows for half of the macrocells to drive I/O cells within a PAL block, in combinations according to Figure 12. Each I/O cell can choose from eight macrocells; each macrocell has a choice of four I/O cells.

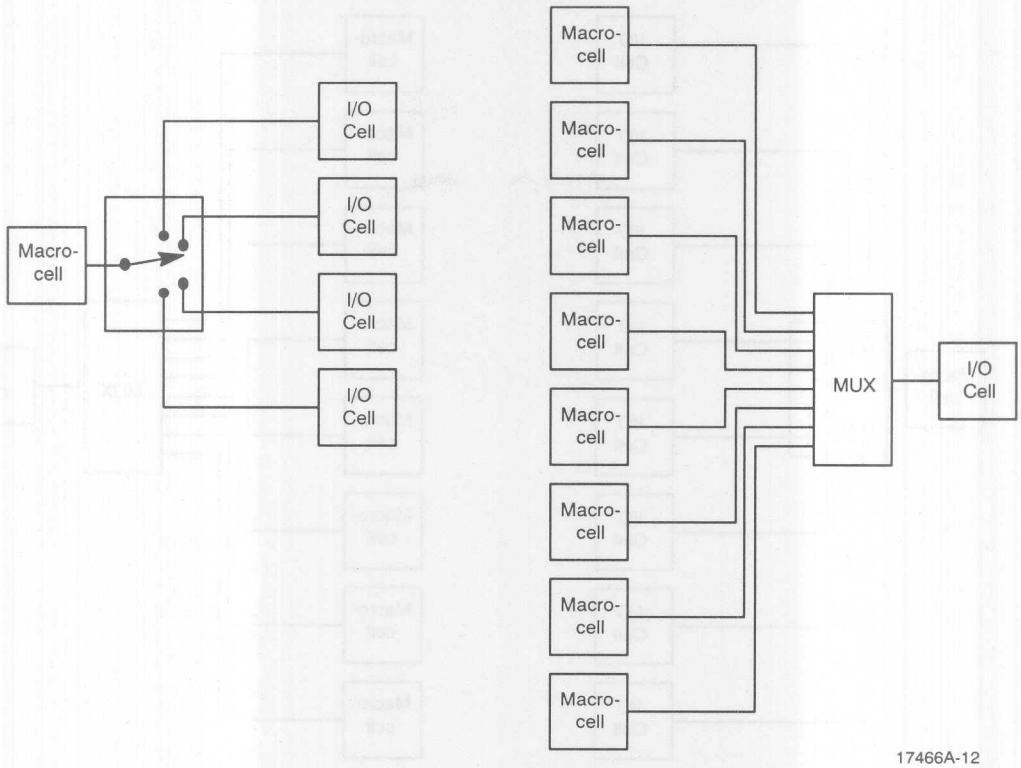
Specific combinations allowed for each device are tabulated in the individual product data sheets. No macrocell may drive more than one I/O cell.



a. Macrocell drives one of 8 I/Os

b. I/O can choose one of 8 macrocells

Figure 11. MACH 3 Output Switch Matrix



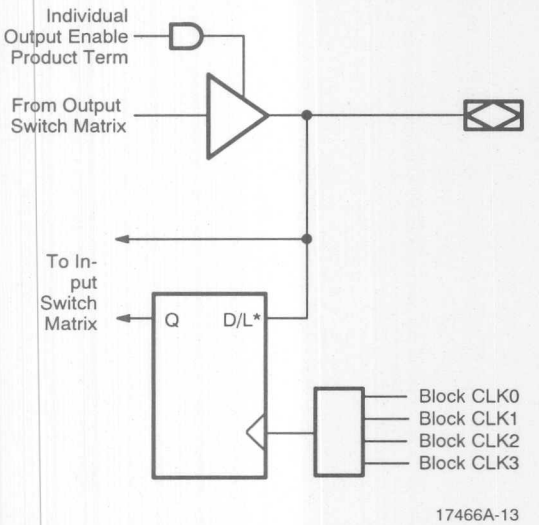
a. Macrocell drives one of 4 I/Os

b. I/O can choose one of 8 macrocells

Figure 12. MACH 4 Output Switch Matrix

The I/O Cell

The I/O cell (Figure 13) simply consists of programmable output enable, a feedback path, and for MACH 4 devices, a flip-flop. An individual output enable product term is provided for each I/O cell. The feedback signal drives the input switch matrix.



**Flip-flop available on MACH 4 devices only.*

Figure 13. I/O Cell

The MACH 4 I/O cell contains a flip-flop, which provides the capability for storing the input in a D-type register or latch. The clock can be any of the PAL block clocks. Both the direct and registered versions of the input are sent to the input switch matrix. This allows for such functions as "time-domain-multiplexed" data comparison, where the first data value is stored, and then the second data value is put on the I/O pin and compared with the previous stored value.

Note that the flip-flop used in the MACH 4 I/O cell is independent of the flip-flops in the macrocells. It powers up to a logic low.

JTAG Testability Circuit

All MACH 3 and 4 devices with greater than 84 leads have JTAG testability circuits built in. This allows functional testing of the device through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

The only device without JTAG is the MACH435, which is pin-compatible with the 84-pin MACH130 and MACH230. This device has preload and observability functions. All registers on the MACH435 can be preloaded to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

In addition to the control offered by preload, testing requires observability of the internal state of the device following a sequence of vectors. The MACH435 offers an observability feature that allows the user to send hidden buried register values to observable output pins.

5-V In-Circuit Programmability and Erasability

Because high-pin-count PQFPs have leads that are subject to damage, 5-V in-circuit programmability and erasability have been provided. This allows the devices to be soldered on the board prior to programming. Once on the board, the device leads are immobile, and can be programmed without damage. Because there are no "supervoltages" (voltages above the standard TTL range), devices that share lines on the board will not be damaged by high voltages. Programming is enabled by a dedicated pin; this pin should be firmly grounded during normal operation.

Power-Up Reset/Preset

All flip-flops power up to a known state for predictable system initialization. The power-up value can be programmed through the initialization swapping/selection feature. The V_{CC} rise must be monotonic and clock must be inactive until the reset delay time, 1000 ns maximum, has elapsed.

Security Bit

A security bit is provided on the MACH devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit, but preload and the JTAG circuitry can be used independently of the security bit. The bit can only be erased in conjunction with the array during an erase cycle.

Quality and Testability

The MACH devices offer a very high level of built-in quality. The fact that the device is erasable allows direct verification of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The MACH devices are fabricated with AMD's advanced electrically-erasable floating-gate 0.65-µm CMOS technology. This provides the devices with performance and power consumption that are unmatched in the industry. The floating gate cells rely on Fowler-Nordheim tunneling to charge the gate, and have long proven their endurance and reliability. 20-year data retention is provided over operating conditions when devices are programmed on approved programmers.

The substrate of these devices is grounded, providing for a more efficient circuit. In addition, this provides substrate clamp diodes at all inputs, making them more immune to noisy input signals. All of the MACH 3 and MACH 4 devices have pull-up resistors on all inputs and I/O pins. While it is good design practice to tie unused pins high, the pull-up resistors allow unused pins to float safely.

PRELIMINARY COM'L: -15/20

MACH435-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **84 pins in PLCC**
- **128 macrocells**
- **15 ns t_{PD}**
- **50 MHz f_{MAX} external**
- **70 inputs with pull-up resistors**
- **64 outputs**
- **192 flip-flops**
  - 128 macrocell flip-flops
  - 64 input flip-flops
- **Up to 20 product terms per function, with XOR**
- **Flexible clocking**
  - four global clock pins with selectable edges
  - asynchronous mode available for each macrocell
- **8 "PAL33V16" blocks**
- **Input and output switch matrices for high routability**
- **Fixed, predictable, deterministic delays**
- **Pin compatible with MACH130, MACH230**

GENERAL DESCRIPTION

The MACH435 is a member of AMD's high-performance EE CMOS MACH 4 family. This device has approximately twelve times the macrocell capability of the popular PAL22V10, with significant density and functional features that the PAL22V10 does not provide.

The MACH435 consists of eight PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The MACH435 has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

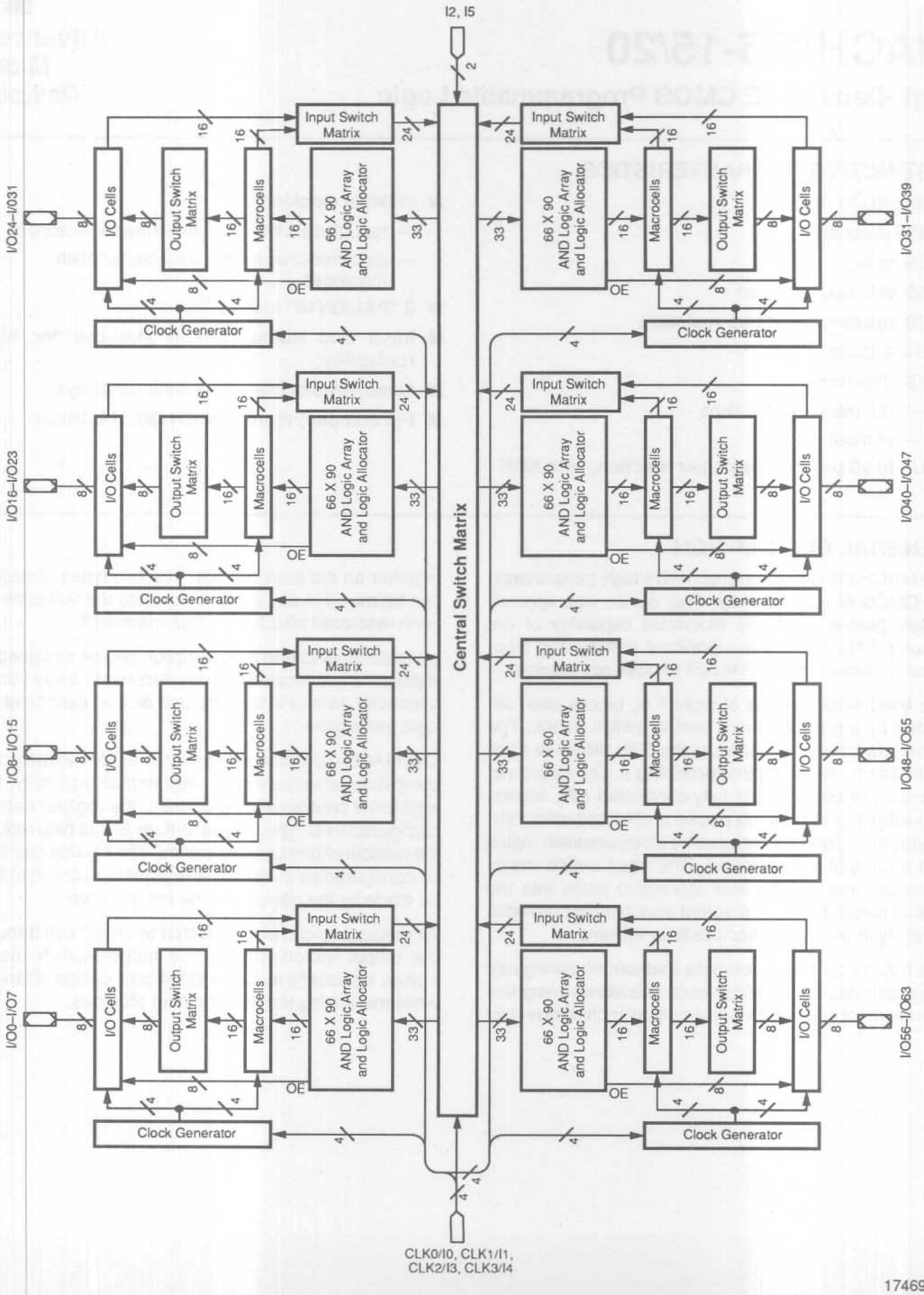
Up to 20 product terms per function can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

The MACH435 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer or by the software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

Publication# 17469 Rev. A Amendment/0
Issue Date: December 1992

BLOCK DIAGRAM



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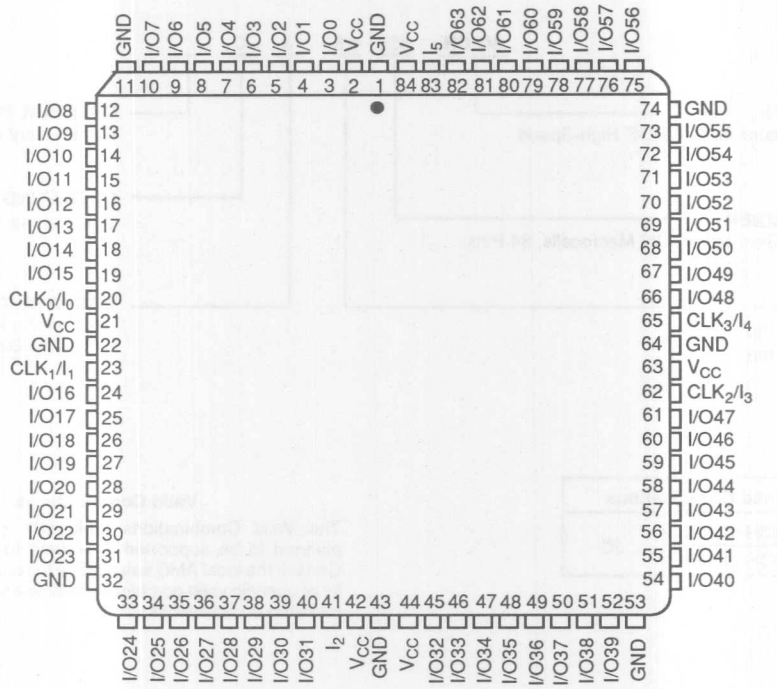
CONNECTION DIAGRAM
Top View

PLCC



17469A-2

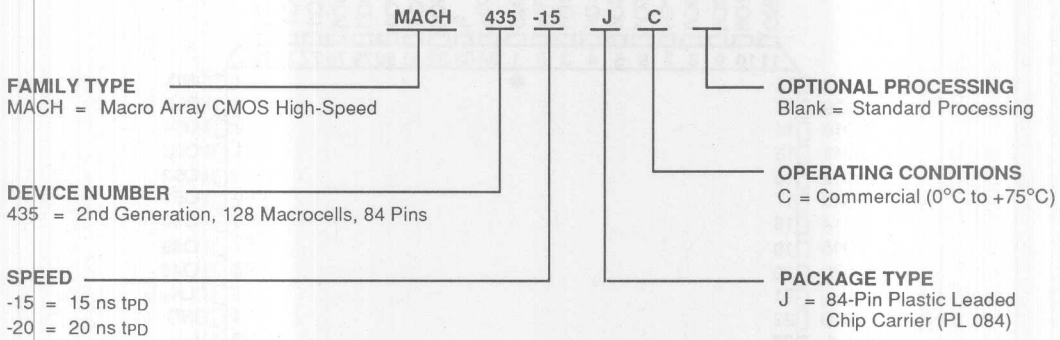
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

Note:
Pin-compatible with MACH130, MACH230

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH435-15	JC
MACH435-20	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH435 consists of eight PAL blocks connected by a central switch matrix. There are 64 I/O pins and 6 dedicated input pins feeding the central switch matrix. These signals are distributed to the eight PAL blocks for efficient design implementation. There are 4 global clock pins that can also be used as dedicated inputs.

All inputs and I/O pins have built-in pull-up resistors. While it is always good design practice to tie unused pins high, the pull-up resistors provide design security and stability in the event that unused pins are left disconnected.

The PAL Blocks

Each PAL block in the MACH435 (Figure 14) contains a clock generator, a 90-product-term logic array, a logic allocator, 16 macrocells, an output switch matrix, 8 I/O cells, and an input switch matrix. The central switch matrix feeds each PAL block with 33 inputs. This makes the PAL block look effectively like an independent "PAL33V16" with 8 to 16 buried macrocells.

In addition to the logic product terms, individual output enable product terms and two PAL block initialization product term are provided. Each I/O pin can be individually enabled. All flip-flops that are in the synchronous mode within a PAL block are initialized together by either of the PAL block initialization product terms.

The Central Switch Matrix and Input Switch Matrix

The MACH435 central switch matrix is fed by the input switch matrices in each PAL block. Each PAL block provides 16 internal feedback signals, 8 registered input signals, and 8 I/O pin signals to the input switch matrix. Of these 32 signals, 24 decoded signals are provided to the central switch matrix by the input switch matrix. The central switch matrix distributes these signals back to the PAL blocks in a very efficient manner that provides for high performance. The design software automatically configures the input and central switch matrices when fitting a design into the device.

The Clock Generator

Each PAL block has a clock generator that can generate four clock signals for use throughout the PAL block. These four signals are available to all macrocells and I/O cells in the PAL block, whether in synchronous or asynchronous mode. The clock generator chooses the four signals from the eight possible signals given by the true and complement versions of the four global clock pin signals. The possible combinations are listed in Table 1 on page 6.

The Product-Term Array

The MACH435 product-term array consists of 80 product terms for logic use, eight product terms for output enable use, and two product terms for global PAL block initialization. Each macrocell has a nominal allocation of 5 product terms for logic, although the logic allocator allows for logic redistribution. Each I/O pin has its own individual output enable term. The initialization product terms provide asynchronous reset or preset to synchronous-mode macrocells in the PAL block.

The Logic Allocator

The logic allocator in the MACH435 takes the 80 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 20 product terms if in synchronous mode, or 18 product terms if in asynchronous mode. When product terms are routed away from a macrocell, it is possible to route all 5 product terms away, which precludes the use of the macrocell for logic generation; or it is possible to route only 4 product terms away, leaving one for simple function generation. The design software automatically configures the logic allocator when fitting the design into the device.

The logic allocator also provides an exclusive-OR gate. This gate allows generation of combinatorial exclusive-OR logic, such as comparison or addition. It allows registered exclusive-OR functions, such as CRC generation, to be implemented more efficiently. It also makes in possible to emulate all flip-flop types with a D-type flip-flop. Register type emulation is automatically handled by the design software.

Table 5 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 14 for cluster and macrocell numbers.

Table 5. Logic Allocation

Macrocell	Available Clusters
M0	C0, C1, C2
M1	C0, C1, C2, C3
M2	C1, C2, C3, C4
M3	C2, C3, C4, C5
M4	C3, C4, C5, C6
M5	C4, C5, C6, C7
M6	C5, C6, C7, C8
M7	C6, C7, C8, C9
M8	C7, C8, C9, C10
M9	C8, C9, C10, C11
M10	C9, C10, C11, C12
M11	C10, C11, C12, C13
M12	C11, C12, C13, C14
M13	C12, C13, C14, C15
M14	C13, C14, C15
M15	C14, C15

The Macrocell and Output Switch Matrix

The MACH435 has 16 macrocells, half of which can drive I/O pins; this selection is made by the output switch matrix. Each macrocell can drive one of four I/O cells. The allowed combinations are shown in Table 6. Please refer to Figure 14 for macrocell and I/O pin numbers.

Table 6. Output Switch Matrix Combinations

Macrocell	Routable to I/O Pins
M0, M1	I/O5, I/O6, I/O7, I/O0
M2, M3	I/O6, I/O7, I/O0, I/O1
M4, M5	I/O7, I/O0, I/O1, I/O2
M6, M7	I/O0, I/O1, I/O2, I/O3
M8, M9	I/O1, I/O2, I/O3, I/O4
M10, M11	I/O2, I/O3, I/O4, I/O5
M12, M13	I/O3, I/O4, I/O5, I/O6
M14, M15	I/O4, I/O5, I/O6, I/O7
I/O Pin	**Available Macrocells**
I/O0	M0, M1, M2, M3, M4, M5, M6, M7
I/O1	M2, M3, M4, M5, M6, M7, M8, M9
I/O2	M4, M5, M6, M7, M8, M9, M10, M11
I/O3	M6, M7, M8, M9, M10, M11, M12, M13
I/O4	M8, M9, M10, M11, M12, M13, M14, M15
I/O5	M10, M11, M12, M13, M14, M15, M0, M1
I/O6	M12, M13, M14, M15, M0, M1, M2, M3
I/O7	M14, M15, M0, M1, M2, M3, M4, M5

The macrocells can be configured as registered, latched, or combinatorial. In combination with the logic allocator, the registered configuration can be any of the standard flip-flop types. The macrocell provides internal feedback whether configured with or without the flip-flop, and whether or not the macrocell drives an I/O cell.

The flip-flop clock depends on the mode selected for the macrocell. In synchronous mode, any of the PAL block clocks generated by the Clock Generator can be used. In asynchronous mode, the additional choice of either edge of an individual product-term clock is available.

Initialization can be handled as part of a bank of macrocells via the PAL block initialization terms if in synchronous mode, or individually if in asynchronous mode. In synchronous mode, one of the PAL block product terms is available each for preset and reset. The swap function determines which product term drives which function. This allows initialization polarity compatibility with the MACH 1 and 2 series. In asynchronous mode, one product term can be used either to drive reset or preset.

The I/O Cell

The I/O cell in the MACH435 consists of a three-state buffer and an input flip-flop. The I/O cell is driven by one of the macrocells, as selected by the output switch matrix. Each I/O cell can take its input from one of eight macrocells. The three-state buffer is controlled by an individual product term. The input flip-flop can be configured as a register or latch. Both the direct I/O signal and the registered/latched signal are available to the input switch matrix, and can be used simultaneously if desired.

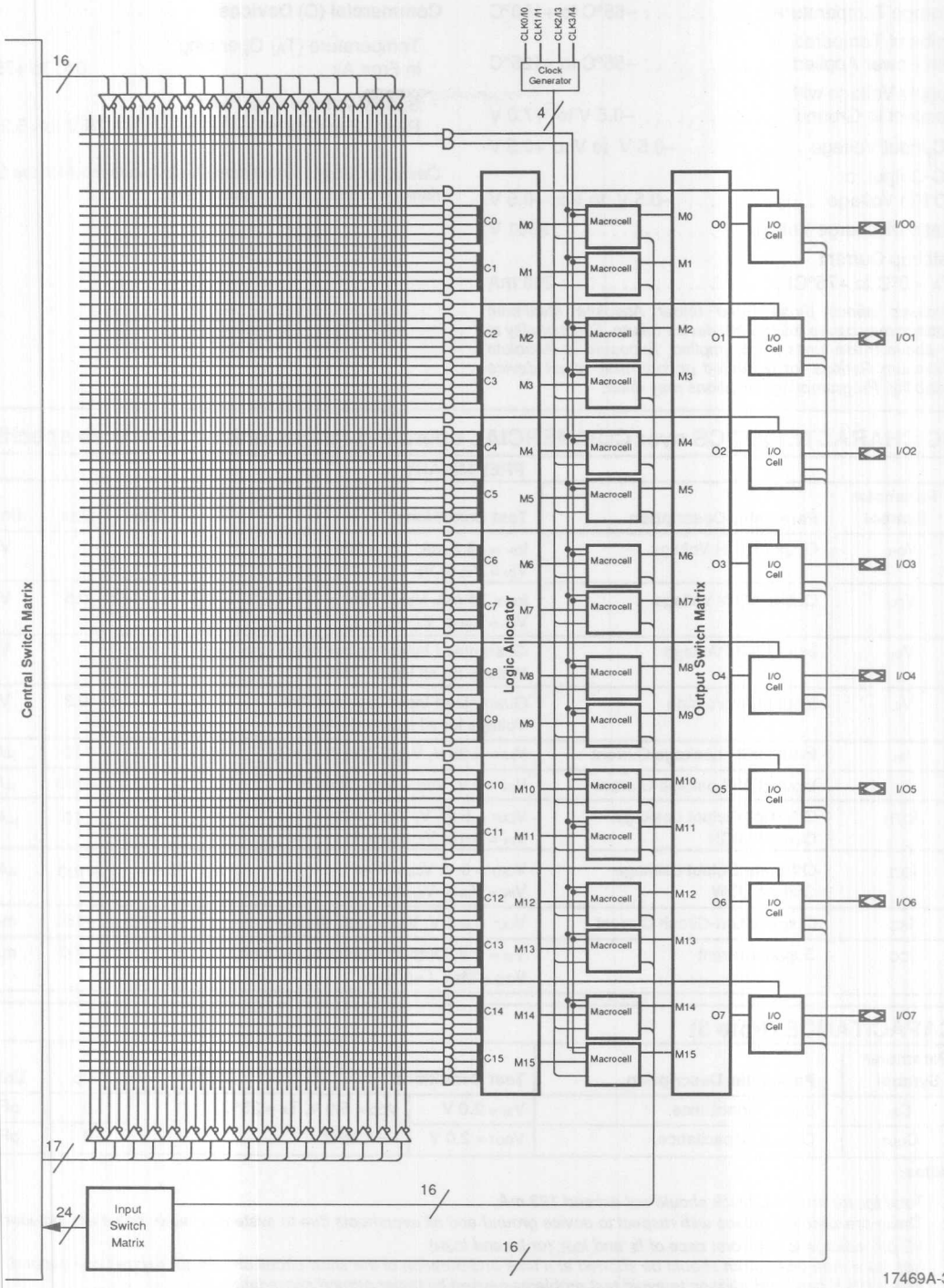


Figure 14. MACH PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} +0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} +0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +75°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30	–160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f =0 MHz		400	mA

CAPACITANCE (Note 5)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

PRELIMINARY

Parameter Symbol	Parameter Description				-15 Min	-15 Max	-20 Min	-20 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 2)				3	15	3	20	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				6		8		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				6		8		ns
t_{COA}	Product Term Clock to Output (Note 3)				4	18	4	22	ns
t_{WLA}	Product Term, Clock Width			LOW	9		12		ns
t_{WHA}				HIGH	9		12		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 3)	External Feedback	$1/(t_{SA} + t_{COA})$		41.7		33.3		MHz
		Internal Feedback (f_{CNTA})							MHz
		No Feedback	$1/(t_{WLA} + t_{WHA})$		55.6		41.7		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock				10		13		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		ns
t_{COS}	Global Clock to Output (Note 3)				2	10	2	12	ns
t_{WLS}	Global Clock Width			LOW	6		8		ns
t_{WHS}				HIGH	6		8		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 3)	External Feedback	$1/(t_{SS} + t_{COS})$		50		40		MHz
		Internal Feedback (f_{CNTS})			66.6		50		MHz
		No Feedback	$1/(t_{WLS} + t_{WHS})$		83.3		62.5		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				6		8		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				6		8		ns
t_{GOA}	Product Term Gate to Output (Note 2)					19		22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				9		12		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate				10		13		ns
t_{HLS}	Latch Data Hold Time Using Global Gate				0		0		ns
t_{GOS}	Gate to Output (Note 3)					11		12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				6		8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					17		22	ns
t_{SIR}	Input Register Setup Time				2		2		ns
t_{HIR}	Input Register Hold Time				2.5		3		ns
t_{ICO}	Input Register Clock to Combinatorial Output					20		25	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

Parameter Symbol	Parameter Description		-15 Min	-15 Max	-20 Min	-20 Max	Unit
t_{ICS}	Input Register Clock to Output Register Setup		15		20		ns
t_{WICL}	Input Register Clock Width	LOW	6		8		ns
t_{WICH}		HIGH	6		8		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time		2		2		ns
t_{HIL}	Input Latch Hold Time		2.5		3		ns
t_{IGO}	Input Latch Gate to Combinatorial Output			20		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			22		27	ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Latch Gate		8		10		ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		12		16		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Global Output Latch Gate		12		16		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		16		21		ns
t_{WIGZ}	Input Latch Gate Width LOW		6		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			19		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 3)		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)		10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			20		25	ns
t_{APW}	Asynchronous Preset Width (Note 3)		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 3)		10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 2)		2	15	2	20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 2)		2	15	2	20	ns

Notes:

1. *See Switching Test Circuit, page 36, for test conditions.*
2. *Parameters measured with 32 outputs switching.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*

MACH355-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 132 pins in PQFP
- 96 macrocells
- 15 ns t_{PD}
- 50 MHz f_{MAX} external
- 102 inputs with pull-up resistors
- 96 outputs
- 96 flip-flops
- Up to 20 product terms per function, with XOR
- Flexible clocking
  - — four global clock pins with selectable edges
  - — asynchronous mode available for each macrocell
- JTAG, 5-V programmability
- 6 "PAL33V16" blocks
- Input and output switch matrices for high routability
- Fixed, predictable, deterministic delays

GENERAL DESCRIPTION

The MACH355 is a member of AMD's high-performance EE CMOS MACH 3 family. This device has approximately nine times the macrocell capability of the popular PAL22V10, with significant density and functional features that the PAL22V10 does not provide.

The MACH355 consists of six PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The MACH355 has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

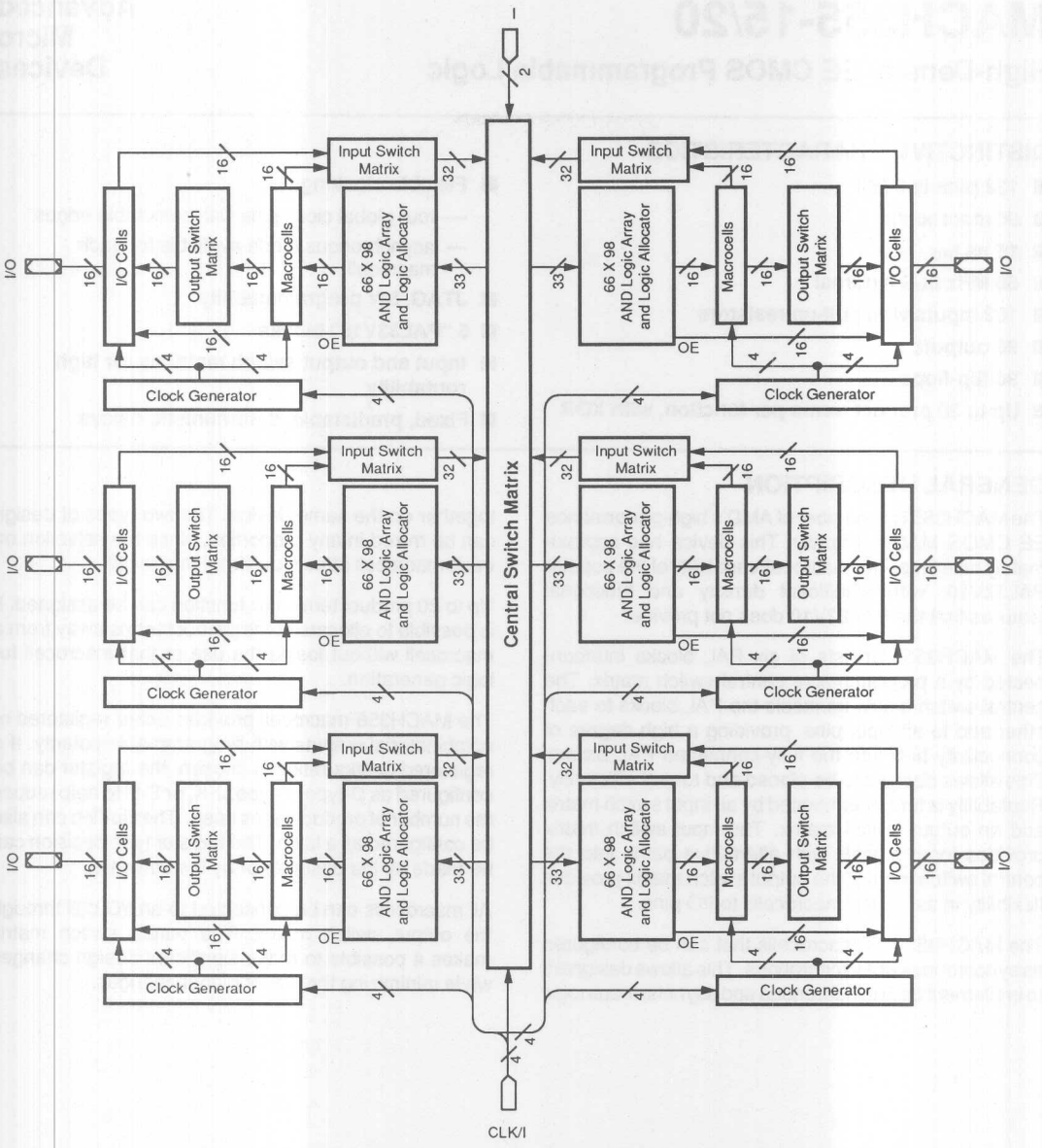
Up to 20 product terms per function can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

The MACH355 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer or by the software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

Publication# 17467 Rev. A Amendment/0
Issue Date: December 1992

BLOCK DIAGRAM



17467A-1

ADVANCE INFORMATION

MACH445-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **100 pins in PQFP**
- **MACH435 with JTAG, 5-V programmability**
- **128 macrocells**
- **15 ns t_{PD}**
- **50 MHz f_{MAX} external**
- **70 inputs with pull-up resistors**
- **64 outputs**
- **192 flip-flops**
  - — 128 macrocell flip-flops
  - — 64 input flip-flops
- **Up to 20 product terms per function, with XOR**
- **Flexible clocking**
  - — four global clock pins with selectable edges
  - — asynchronous mode available for each macrocell
- **8 "PAL33V16" blocks**
- **Input and output switch matrices for high routability**
- **Fixed, predictable, deterministic delays**
- **JEDEC-file compatible with MACH435**

GENERAL DESCRIPTION

The MACH445 is a member of AMD's high-performance EE CMOS MACH 4 family. This device has approximately twelve times the macrocell capability of the popular PAL22V10, with significant density and functional features that the PAL22V10 does not provide. It is architecturally identical to the MACH435, with the addition of JTAG and 5-V programmability capabilities.

The MACH445 consists of eight PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The MACH445 has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

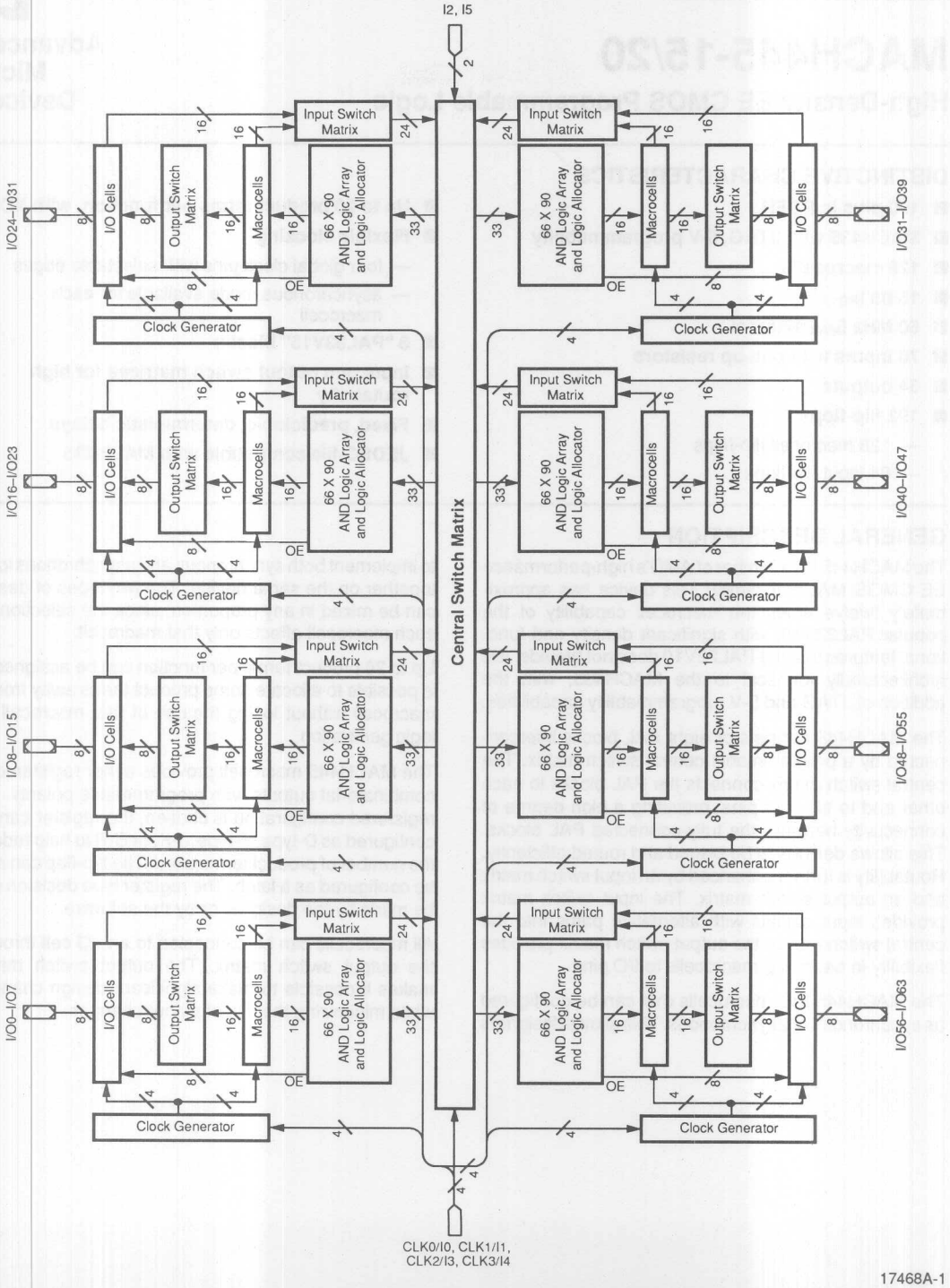
Up to 20 product terms per function can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

The MACH445 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer or by the software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

Publication# 17468 Rev. A Amendment /0
Issue Date: December 1992

BLOCK DIAGRAM



17468A-1

MACH465-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 196 pins in PQFP
- 256 macrocells
- 15 ns t_{PD}
- 50 MHz f_{MAX} external
- 146 inputs with pull-up resistors
- 128 outputs
- 384 flip-flops
  - — 256 macrocell flip-flops
  - — 128 input flip-flops
- Up to 20 product terms per function, with XOR
- Flexible clocking
  - — four global clock pins with selectable edges
  - — asynchronous mode available for each macrocell
- 16 "PAL34V16" blocks
- JTAG, 5-V programmability
- Input and output switch matrices for high routability
- Fixed, predictable, deterministic delays

GENERAL DESCRIPTION

The MACH465 is a member of AMD's high-performance EE CMOS MACH 4 family. This device has approximately 25 times the macrocell capability of the popular PAL22V10, with significant density and functional features that the PAL22V10 does not provide.

The MACH465 consists of 16 PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The MACH465 has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

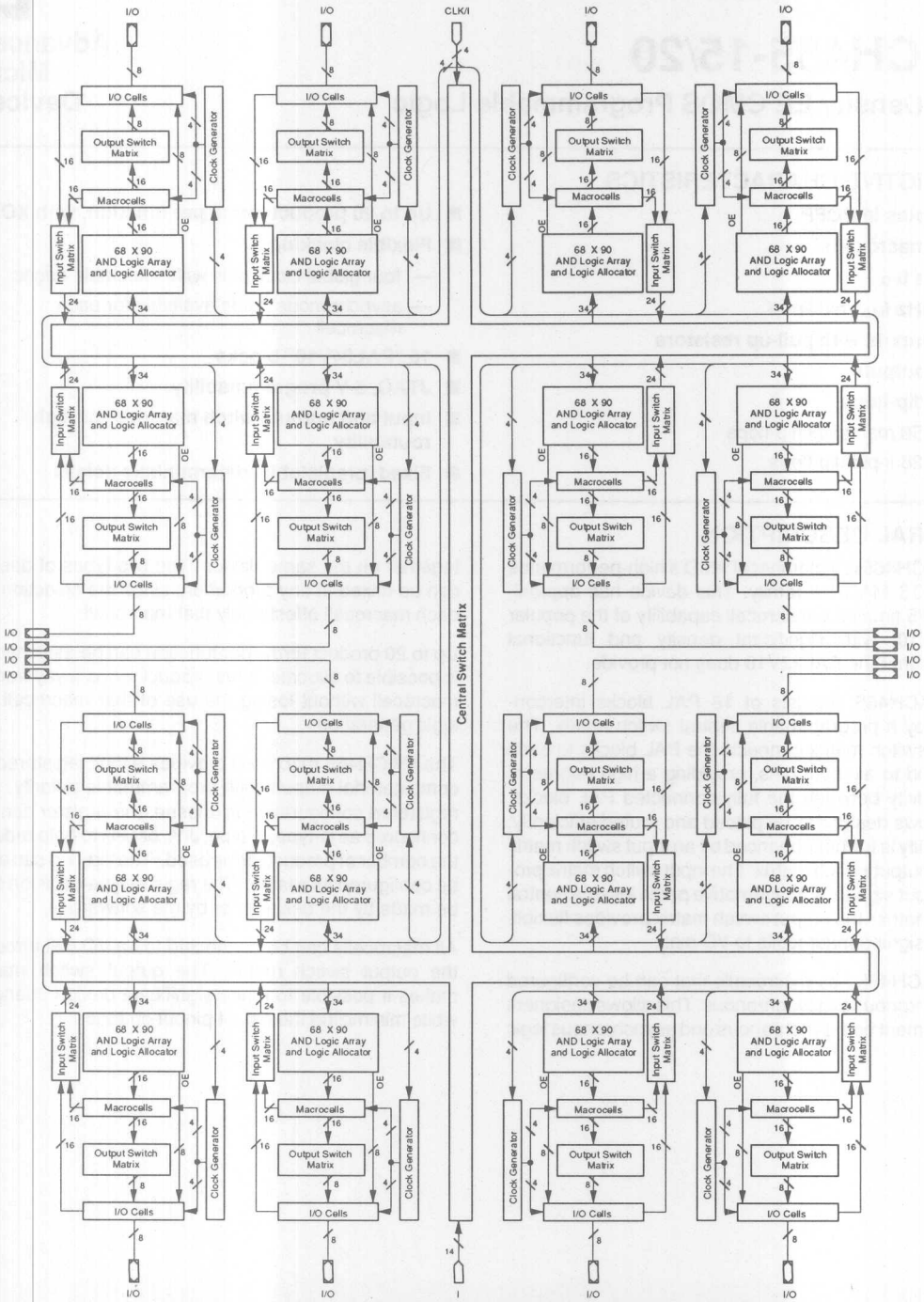
Up to 20 product terms per function can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

The MACH465 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer or by the software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

Publication# 17470 Rev. A Amendment/0
Issue Date: December 1992

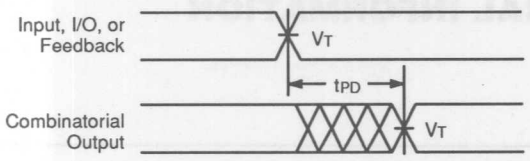
BLOCK DIAGRAM



17470A-1

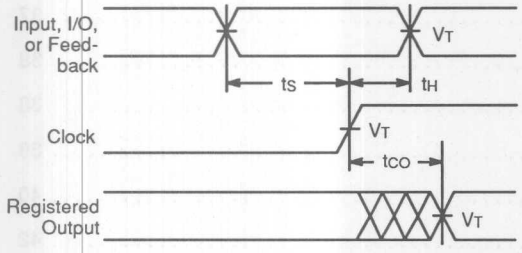
GENERAL INFORMATION

SWITCHING WAVEFORMS



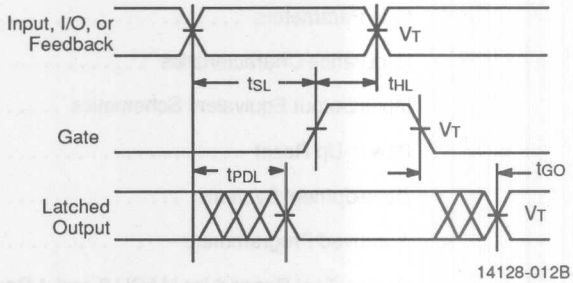
14128-010B

Combinatorial Output



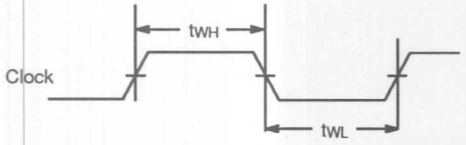
14128-011B

Registered Output



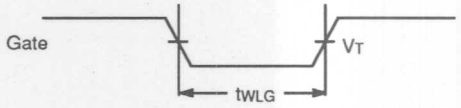
14128-012B

Latched Output



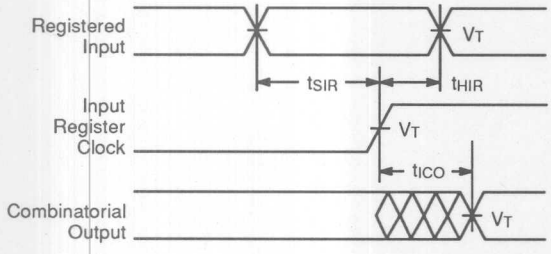
12015-011A

Clock Width



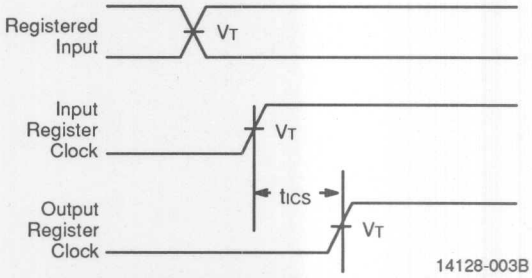
14128-014A

Gate Width



14128-002B

Registered Input



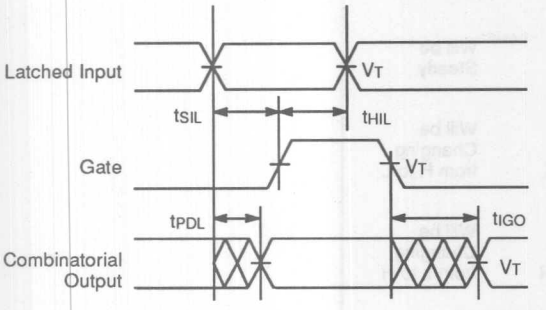
14128-003B

Input Register to Output Register Setup

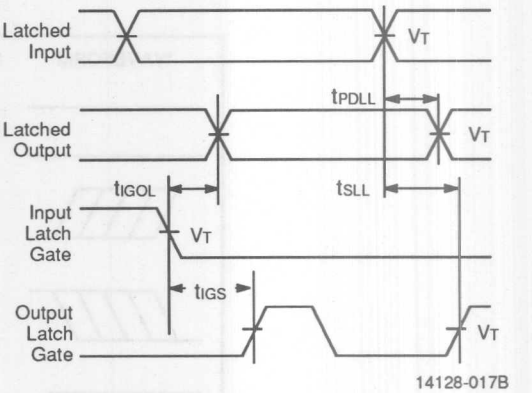
Notes:

1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2–4 ns typical.*

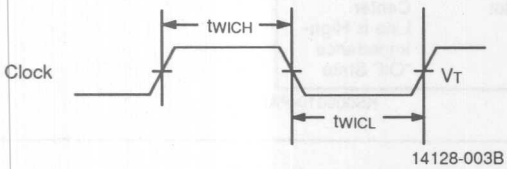
SWITCHING WAVEFORMS



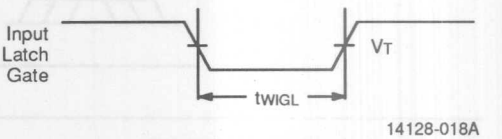
Latched Input



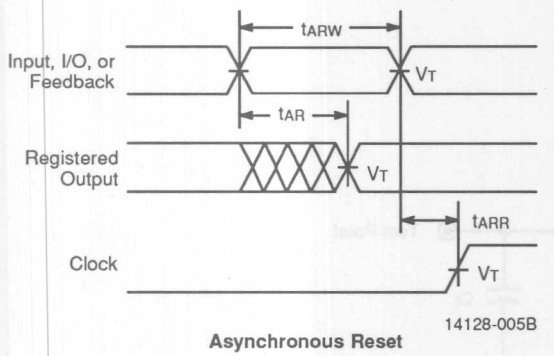
Latched Input and Output



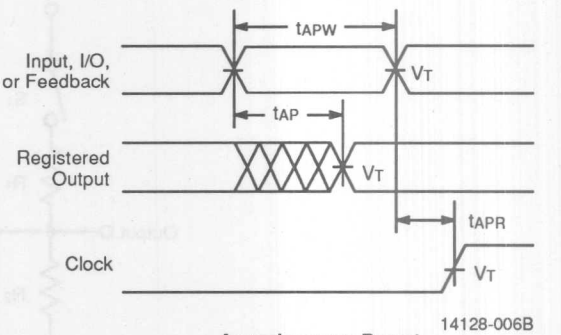
Input Register Clock Width



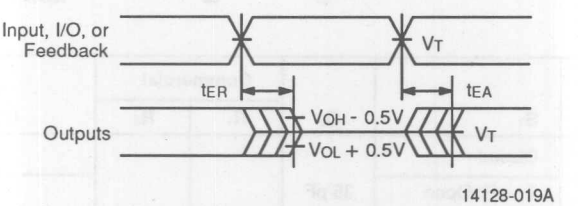
Input Latch Gate Width



Asynchronous Reset



Asynchronous Preset



Output Disable/Enable

Notes:

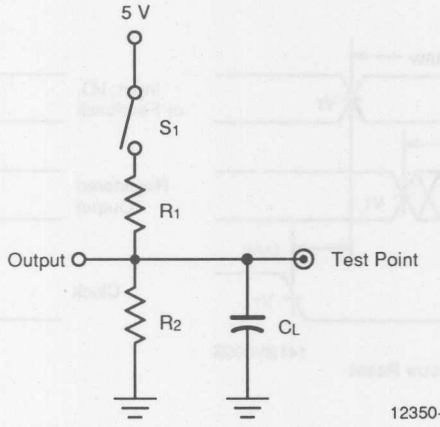
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2–4 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



12350-019A

Specification	S_1	C_L	Commercial R_1	Commercial R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	35 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

f_{MAX} PARAMETERS

The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

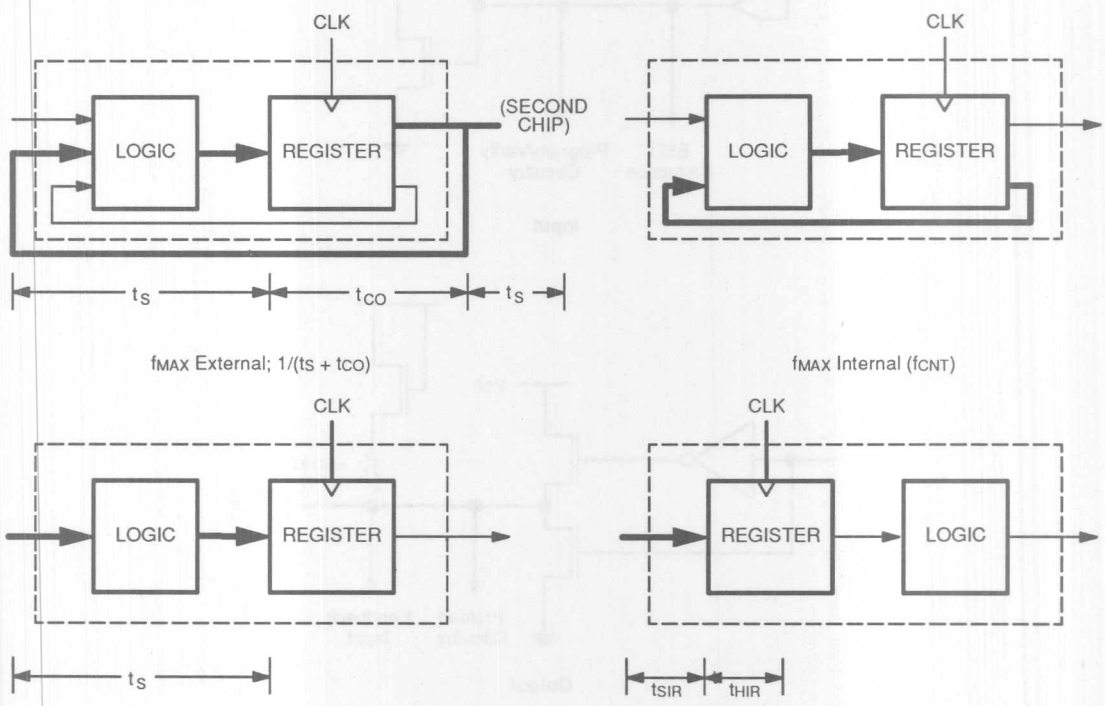
The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external."

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal". A simple internal counter is a good example of this type of design; therefore, this parameter is sometimes called "f_{CNT}."

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback."

For devices with input registers, one additional f_{MAX} parameter is specified: f_{MAXIR}. Because this involves no feedback, it is calculated the same way as f_{MAX} no feedback. The minimum period will be limited either by the sum of the setup and hold times ($t_{SIR} + t_{HIR}$) or the sum of the clock widths ($t_{WICL} + t_{WICH}$). The clock widths are normally the limiting parameters, so that f_{MAXIR} is specified as $1/(t_{WICL} + t_{WICH})$. Note that if both input and output registers are use in the same path, the overall frequency will be limited by t_{ICS}.

All frequencies except f_{MAX} internal are calculated from other measured AC parameters. f_{MAX} internal is measured directly.



12350-023B

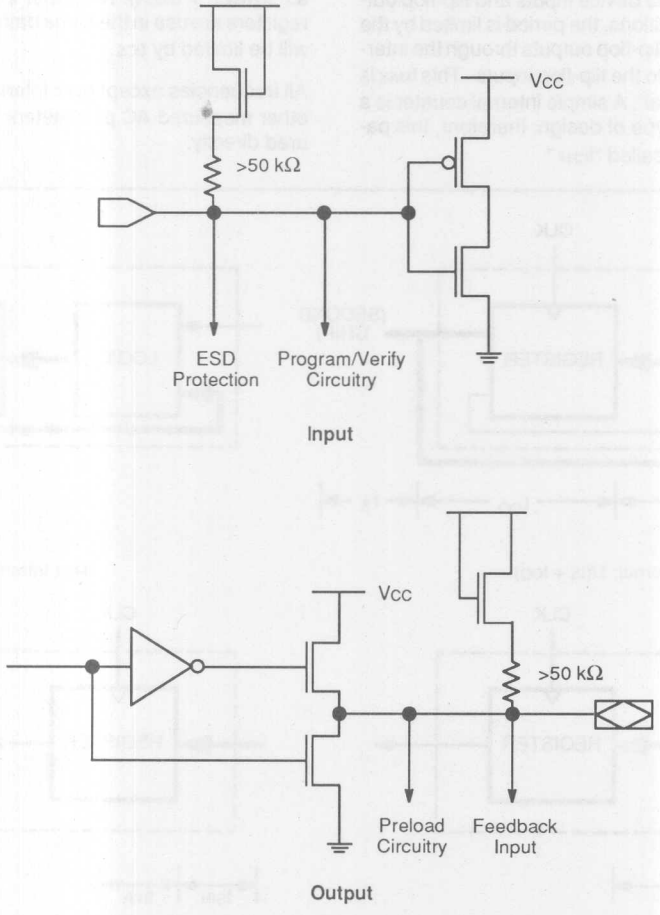
ENDURANCE CHARACTERISTICS

The MACH 3 and MACH 4 families are manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed, a feature which allows 100% testing at the factory.

Endurance Characteristics

Parameter Symbol	Parameter Description	Min	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature (Military)
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



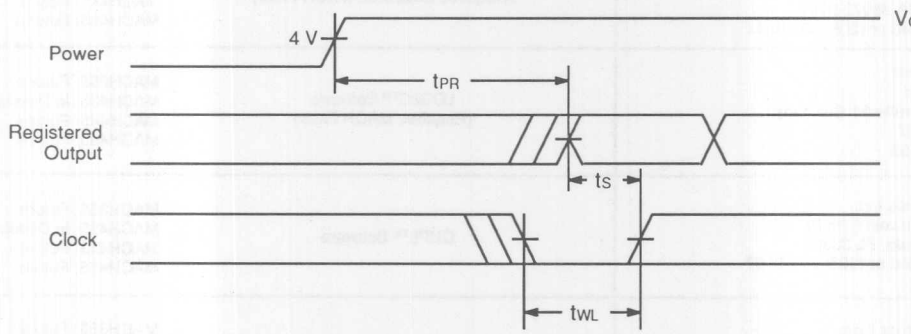
12197-013A

POWER-UP RESET

The MACH devices have been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Max	Unit
t_{PR}	Power-Up Reset Time	10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



12350-024A

Power-Up Reset Waveform

DEVELOPMENT SYSTEMS (subject to change)

For more information on the products listed below, please consult the AMD FusionPLD catalog.

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEM	
Advanced Micro Devices, Inc. 901 Thompson Place MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	MACHXL™ Software	MACH355: Future MACH435: Rev. 1.0 MACH445: Future MACH465: Future
Cadence Design Systems 555 River Oaks Pkwy San Jose, CA 95134 (408) 943-1234	ComposerPLD™ Option (Requires SmartPart™ MACH Fitter) SystemPGA™	MACH355: Future MACH435: Future MACH445: Future MACH465: Future
Capilano Computing 960 Quayside Dr., Suite 406 New Westminster, B.C. Canada V3M 6G2 (800) 444-9064 or (604) 552-6200	MacABEL™ Software (Requires SmartPart MACH Fitter)	MACH355: Future MACH435: In Development MACH445: Future MACH465: Future
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	ABEL™ Software (Requires SmartPart MACH Fitter)	MACH355: Future MACH435: In Development MACH445: Future MACH465: Future
ISDATA GmbH Daimlerstr. 51 W7500 Karlsruhe 21 Germany 0721/75 10 87 (510) 531-8553	LOG/iC™ Software (Requires MACH Fitter)	MACH355: Future MACH435: In Development MACH445: Future MACH465: Future
Logical Devices Inc. 1201 E. Northwest 65th Pl. Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	CUPL™ Software	MACH355: Future MACH435: In Development MACH445: Future MACH465: Future
Mentor Graphics Corp. 8005 S.W. Boeckman Rd. Wilsonville, OR 97070-7777 (800) 547-3000 or (603) 685-7000	PLDSynthesis™	MACH355: Future MACH435: Future MACH445: Future MACH465: Future
MINC Incorporated 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (719) 590-1155	PLDesigner™-XL Software	MACH355: Future MACH435: In Development MACH445: Future MACH465: Future
OrCAD 3175 N.W. Aloclek Dr. Hillsboro, OR 97124 (503) 690-9881	Programmable Logic Design Tools Schematic Design Tool	MACH355: Future MACH435: In Development MACH445: Future MACH465: Future
Viewlogic Systems, Inc. 293 Boston Post Road West Marlboro, MA 01752 (800) 442-4660 or (504) 480-0881	ViewPLD Synthesis (Requires SmartPart MACH Fitter)	MACH355: Future MACH435: Future MACH445: Future MACH465: Future

DEVELOPMENT SYSTEMS (subject to change) (continued)

MANUFACTURER	BOARD-LEVEL SIMULATION PACKAGE	
Aldec Company, Inc. 3525 Old Conejo Rd., Suite 111 Newbury Park, CA 91320 (805) 499-6867	SUSIE™	MACH355: Future MACH435: In Development MACH445: Future MACH465: Future
Cadence Design Systems 555 River Oaks Pkwy San Jose, CA 95134 (408) 943-1234	Models available through Logic Modeling	
Logic Modeling 19500 NW Gibbs Dr. P.O. Box 310 Beaverton, OR 97075 (503) 690–6900	SmartModel® Library	MACH355: Future MACH435: Future MACH445: Future MACH465: Future
OrCAD 3175 N.W. Aloclek Dr. Hillsboro, OR 97124 (503) 690-9881	Digital Simulation Tools (Requires OrCAD/MOD)	MACH355: Future MACH435: Future MACH445: Future MACH465: Future
Teradyne EDA 321 Harrison Ave. Boston, MA 02118 (800) 777-2432 or (617) 422-2793	MultiSIM Interactive Simulator LASAR	MACH355: Future MACH435: Future MACH445: Future MACH465: Future
Viewlogic Systems, Inc. 293 Boston Post Road West Marlboro, MA 01752 (800) 442-4660 or (504) 480-0881	ViewSim Models available through Logic Modeling	
MANUFACTURER	**TEST GENERATION SYSTEM**	
Acugen Software, Inc. 427-3 Amherst St., Suite 391 Nashua, NH 03063 (603) 891-1995	ATGEN™ Test Generation Software	MACH355: Future MACH435: Future MACH445: Future MACH465: Future

Advanced Micro Devices is not responsible for any information relating to the products of third parties. The inclusion of such information is not a representation nor an endorsement by AMD of these products.

APPROVED PROGRAMMERS (subject to change)

For more information on the products listed below, please consult the AMD FusionPLD catalog.

MANUFACTURER	PROGRAMMER CONFIGURATION
Advin Systems, Inc. 1050-L East Duane Ave. Sunnyvale, CA 94086 (408) 243-7000	Contact Manufacturer
BP Microsystems 10681 Haddington, Suite #190 Houston, TX 77043 (800) 225-2102 or (713) 461-9430	CP-1128/PLD-1128 (Note 1) MACH355: Future MACH435: In Development MACH445: Future MACH465: Future
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	MACH355: Future MACH435: In Development MACH445: Future MACH465: Future
Logical Devices Inc. 1201 E. Northwest 65th Pl. Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	MACH355: Future MACH435: In Development MACH445: Future MACH465: Future
Microprоss Parc d'Activite des Pres 5, rue Denis-Papin 59650 Villeneuve-d'Ascq, France (20) 47.90.40	Contact Manufacturer
SMS North America, Inc. 16522 NE 135th Place Redmond, WA 98052 (800) 688-3122 or (214) 233-3122 or SMS Im Morgental 13 D-8994 Hergatz, Germany 07522-5018	MACH355: Future MACH435: In Development MACH445: Future MACH465: Future
Stag Microsystems Inc. 1600 Wyatt Dr. Suite 3 Santa Clara, CA 95054 (408) 988-1118 or Stag House Martinfield, Welwyn Garden City Herfordshire UK AL7 1JT 707-332148	Contact Manufacturer
System General 244 S. Hillview Dr. Milpitas, CA 95035 (408) 263-6667 or 3F, No. 1, Alley 8, Lane 45 Bao Shing Rd., Shin Diau Taipei, Taiwan 2-917-3005	Contact Manufacturer

Note:

1. Requires socket adapter.

PROGRAMMER SOCKET ADAPTERS (subject to change)

MANUFACTURER	PART NUMBER
Emulation Technology 2344 Walsh Ave., Bldg. F Santa Clara, CA 95051 (408) 982–0660	MACH435: (84-Pin to 28-Pin) PLCC: AS-84-28-01P-6
Procon Technologies, Inc. 1333 Lawrence Expwy, Suite 207 Santa Clara, CA 95051 (408) 246-4456	MACH435: (84-Pin to 28-Pin) PLCC: 325-084-1221-028A

Design Tool Support for MACH 3 and 4 Devices

Advanced Micro Devices

DESIGN TOOL SUPPORT STRATEGY

AMD's design tool support strategy for MACH 3 and 4 devices allows users to design with these devices using software and programming tools they already own, at little or no additional cost. This means that designers can complete a design from start to finish in their favorite third-party tools, without having to export the design to an IC-vendor's software package for placement and routing. Because AMD has chosen to establish close engineering and marketing relationships with leading third-party vendors, designers have access to affordable, high-quality support tools for AMD MACH devices at market introduction.

AMD also offers its own low-cost integrated CAE tool for designing with MACH 3 and 4 devices—MACHXL™ software. MACHXL software fully exploits the density and flexibility of MACH 3 and 4 family architectures while providing a low-cost software environment for PC-386/486 and Sun platforms. It is a complete design environment offering text design entry, automatic design rule checking, logic synthesis, hands-off partitioning, placement and routing, JEDEC output, reports on fitting results, and functional simulation in a low-cost PC-386/486-based design environment. For more information on MACHXL software and its planned enhancements, see the following pages in this section.

THIRD-PARTY SUPPORT FOR MACH 3 AND 4 DEVICES

AMD's FusionPLD℠ partners are a select group of leading third-party vendors of support tools with proven track records. Actual development work with these vendors began far in advance of AMD's introduction of MACH 3 and 4 devices. Each FusionPLD partner providing support for these devices adheres to AMD's strict quality and certification requirements. The end result is timely support of new AMD MACH devices on a large number of platforms, as well as a variety of alternative fitters for MACH devices. Support for MACH 3 and 4 devices is available from these leading third-party vendors at no or little additional cost.

Third-party support for MACH 3 and 4 devices is classified as:

- Logic compilers
- CAE environments
- Timing simulation and modeling
- Programmers

Manufacturers of third-party compilers for MACH 3 and 4 devices include Data I/O, MINC, OrCAD, Logical Devices, and ISDATA. These logic compilers typically support MACH 3 and 4 devices through an add-on option to a base software package. This add-on option, named the "MACH Fitter", performs the placement and routing steps completely within the third-party software environment. Some third-parties, such as Data I/O and MINC to date, have developed their own MACH 3 and 4 device Fitter for their respective design environments (ABEL™ 4 and PLDesigner™-XL). Others, such as OrCAD, ISDATA and Logical Devices, may market an AMD-developed MACH Fitter. In all cases, support for MACH 3 and 4 devices is available from these vendors through an add-on MACH Fitter at little or no additional cost.

Support for MACH 3 and 4 devices in CAE environments such as Cadence (and Valid), Mentor and Viewlogic will be available in 1993 through existing OEM and other sales arrangements these companies have made with AMD FusionPLD partners. Again, support for MACH 3 and 4 devices will be available from these vendors or their OEM partners at little or no additional cost.

Timing simulation and modeling support for MACH 3 and 4 devices will be offered by Logic Modeling in first quarter 1993. OrCAD will also support MACH 3 and 4 devices.

Programming support will be available from programmer manufacturers such as Advin, BP Microsystems, Data I/O, Logical Devices, SMS Sprint, and other manufacturers. For a list of software tools and programmers supporting MACH 3 and 4 devices, see the table in the back of this data book.

Publication# 17573 Rev. A Amendment /0
Issue Date: December 1992

AMD'S MACHXL SOFTWARE

General Description

MACHXL software is an integrated CAE tool for designing logic for AMD's MACH 3 and 4 family of devices. It fully exploits the density and flexibility of MACH 3 and 4 family architectures while providing a low-cost software environment. It is similar to AMD's PALASM® 4 software for AMD PAL, MACH 1, and MACH 2 devices.

Features of MACHXL software include:

- Boolean equation design entry
- State machine design entry
- Accepts PALASM 4 design files
- Automatic design rule checking
- Sum of products and XOR optimization
- XOR and register mapping
- Automatic, hands-off partitioning, placement and routing
- Manual intervention controls for fine-tuning partitioning, placement and routing
- JEDEC output
- Easy-to-read reports from the partitioning, placement and routing process
- Functional unit-delay simulation
- PC-386-based design environment
- Low-cost

Future releases will include:

- Schematic interfaces to OrCAD and Viewlogic
- EDIF 2.0 interface
- VERILOG to MACHXL translator
- Support for Microsoft Windows 3.1 environments

System Requirements

MACHXL software can be run on 386 and 486 IBM PC compatibles. The recommended system configuration is:

- IBM PC 386 compatible or greater
- EGA or higher resolution for display
- 8 Mbytes of RAM
- 40 Mbytes hard disk
- DOS 5.0 or later

MACHXL software will be available for Microsoft Windows 3.1 and Sun environments in mid-1993. Contact your local AMD sales office for the latest status information.

MACHXL software for PC-386 systems is not supported under Digital Research's DR-DOS or in networked environments.

User Interface

MACHXL software is a menu-based system, with six main menus:

- FILE
- EDIT
- RUN
- VIEW
- DOWNLOAD
- DOCUMENTATION

The FILE menu allows users to create new designs, retrieve existing designs, modify the system settings for compilation, simulation and logic synthesis, change directories, and gives them access to the operating system.

Use the EDIT menu to bring up a text design or auxiliary simulation file for editing.

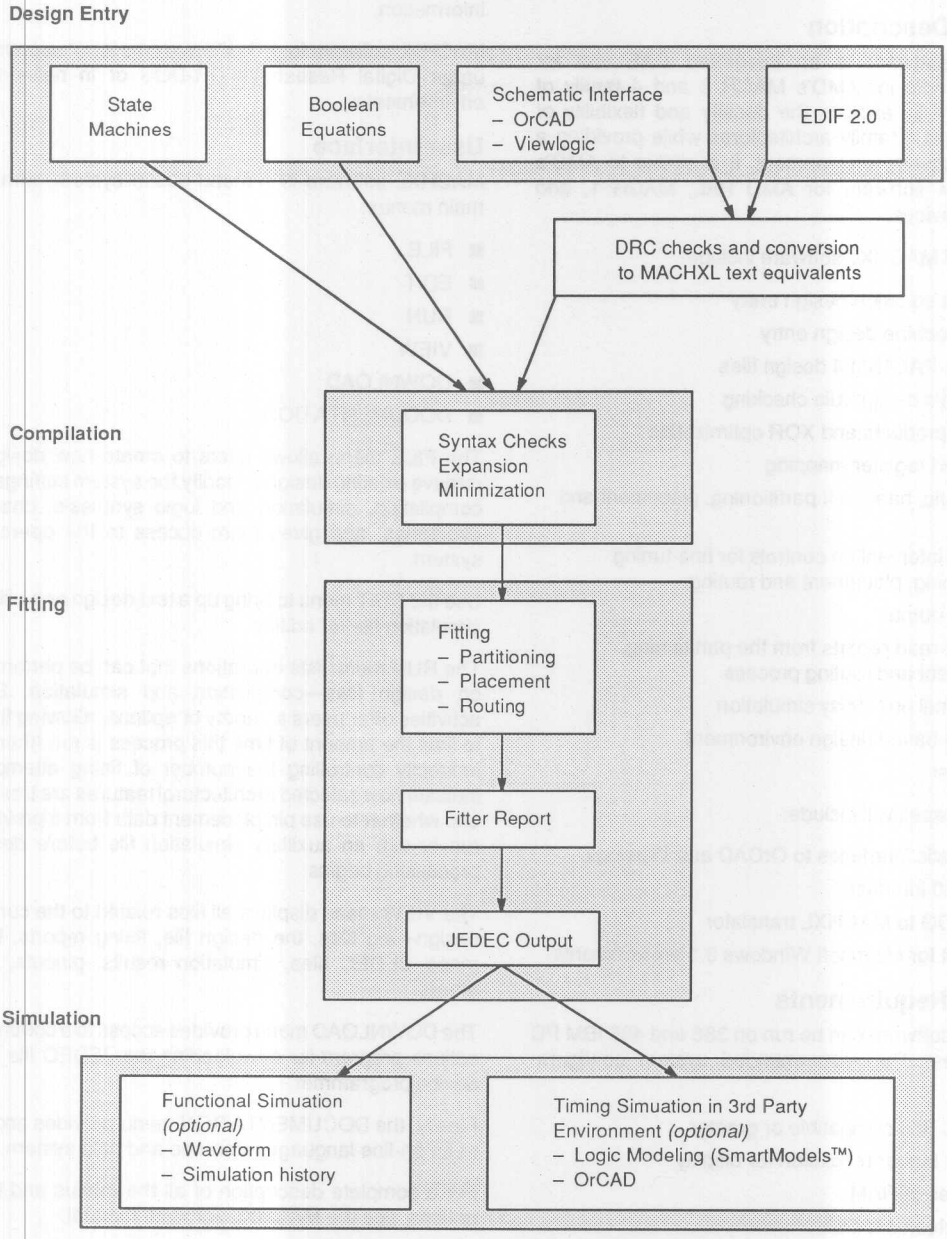
The RUN menu lists operations that can be performed on design files—compilation and simulation. Both activities offer users a variety of options, allowing them to limit the amount of time this process is run (thereby indirectly controlling the number of fitting attempts), indicate how selected architectural features are treated, and whether to use pin placement data from a previous run or use an auxiliary simulation file before design processing begins

The VIEW menu displays all files related to the current design—log files, the design file, fitting reports, fuse maps, JEDEC files, simulation results, pinouts, and others.

The DOWNLOAD menu provides access to a communications program for downloading the JEDEC file to a device programmer.

Finally, the DOCUMENTATION menu provides access to an on-line language reference and help system.

For a complete description of all the menus and their options, see the MACHXL software manual.


Design Entry
State Machines
Boolean Equations
Schematic Interface
– OrCAD
– Viewlogic
EDIF 2.0
DRC checks and conversion to MACHXL text equivalents
Compilation
Syntax Checks
Expansion
Minimization
Fitting
Fitting
– Partitioning
– Placement
– Routing
Fitter Report
JEDEC Output
Simulation
Functional Simuation
(optional)
– Waveform
– Simulation history
Timing Simuation in 3rd Party Environment (optional)
– Logic Modeling (SmartModels™)
– OrCAD

17573A-1

Design Entry

Initially, MACHXL software design entry methods will be limited to Boolean equations and state machines. MACHXL software will also accept PALASM 4 design files.

In mid-1993, design entry capabilities will be expanded, adding schematic and EDIF interfaces to popular schematic editors and CAE tools such as OrCAD and Viewlogic. A Verilog-to-MACHXL translator, and a JEDEC-to-VERILOG translator are also in development.

Compilation

During compilation, MACHXL software reads the target device type, the pin and node signal information, and the design description before performing design rule and resource checks. During design rule checking, the software takes the signal declarations in the pin/node list and the information on which signals are to be used as inputs, outputs, and/or buried nodes, and combines it with any information on which pins those signals are to be located on, before performing a series of checks. Finally, the software informs the user of any design inconsistencies.

Fitting

AMD designed the MACHXL Fitter technology for MACH 3 and 4 devices with three goals in mind:

- Hands-off automatic routing for 100% of designs with all pins are fixed, if a fit exists
- Hands-off automatic routing for 90% of designs with all pins floating, if a fit exists
- 100% routability for designs with up to 80% utilization

To accomplish these goals, AMD has endowed the MACHXL Fitter with knowledge of optimal partitioning techniques in order to place and route signals to the appropriate blocks through the multiple switch matrices without manual intervention. Manual intervention is required only for the most difficult designs.

During partitioning (one of the most important phases of fitting) equations are partitioned into blocks after checking the block constraints on set/reset, product term clusters, product term steering, XOR, array inputs, clocks and pins. An intelligent seed selection allows the software to partition equations into different blocks while minimizing interconnections between blocks and maximizing the amount of logic that can be fitted.

During placement, macrocells, pin and node numbers are assigned to output signals and input variables after checking device resource requirements (product terms, XOR, clocks) and any pre-placed pins. Each macrocell is configured for either asynchronous or synchronous operation. Product terms are also synthesized by converting them into product term clusters, XOR gates, etc. as required. The placement software accommodates designs with all pins floating, pre-placed signals, or a mixture of pre-placed and floating signals.

After placement, the MACHXL router attempts to match the placed signals through the input, output and central switch matrix to the blocks that reference them. If no match is found, then a new placement is generated based on information returned by the router.

Designs are automatically fitted by the MACHXL software into MACH 3 and 4 devices in minutes. The fitter will attempt multiple placements until one is found that routes, or until the user-specified time limit is reached.

Fitting Options for Manual Intervention

As stated earlier, the goals of the MACHXL Fitter technology for MACH 3 and 4 devices are to provide hands-off automatic routing for 90% of floating-pin designs, and 100% of fixed-pin designs. In fixed-pin designs, pre-placing pins and nodes in the design file will force the Fitter to use the specified pinout when the design is changed or additional logic is added. Other fitting options in the MACHXL software help the user maximize the amount of logic placed in the device and/or its performance.

Fitter partitioning is strongly affected by the number of wires connecting logic functions placed in different blocks. In order to fit, a portion of logic cannot exceed the resources of a block, and for synchronous applications, must share common set and reset signals. Users can manually control this crucial Fitter partitioning process by pre-placing portions of logic in specific blocks using the GROUP command. This MACHXL command allows users to group signals sharing many logic variables and pre-place them in certain blocks. This aids the Fitter in partitioning blocks and reducing routing congestion.

Another MACHXL syntax element that aids manually directed fitting of MACH 3 and 4 devices is the PAIR keyword, an optional attribute for pin or node statements that directs input or output pairing. Input pairing logically associates an input pin with an input register; output pairing associates nodes with an output pin. Pairing allows the MACHXL software to treat the input/output pin and it's associated node as a single entity during fitting, aiding resource assignment, and reducing routing congestion and/or redundant equations.

Logic synthesis options, such as automatic pin/node pairing, and automatic gate splitting of larger logic equations into smaller clusters with fewer product terms also aid in optimizing resource utilization or performance. For more information, see the MACHXL software manual.

REPORT FILES

The report output files list compilation error messages and detail the resources used. The MACHXL software report file shows the results of mapping the design to the device resources:

- Device Resource Checks – displays device resource utilization.
- Timing Analysis – displays minimum and maximum delay paths.
- Block Partitioning – displays utilization by block.
- Signals Tabular Form – depicts how the logic is mapped onto physical macrocells and the interconnect provided by the switch matrix.

The information in these files can also be used to determine if additional logic can be added, where it can be added, and what logic, if any, should be removed in case of a no-fit. The MACHXL software manual explains in greater detail how to use these report files to maximize MACH 3 and 4 device utilization.

Simulation

MACHXL software provides a simple unit delay simulator that allows users to verify their designs. Simulation results can be viewed as waveforms for easy analysis. Simulation commands can be defined in either the simulation segment of the design file or in an auxiliary simulation file.

Simulation options in MACHXL software allow designers to use an auxiliary simulation file, and to specify the source of the data for signal placement—the last successful placement, a previously saved placement, or the design file.

For those MACHXL software users planning to create timing models, a JEDEC-to-VERILOG translator is also planned for release in 1993.

Generating the JEDEC File

MACHXL software generates a JEDEC file for programming the MACH 3 and 4 devices. These devices can be programmed on industry standard PLD programmers with the appropriate personality and socket adapters. See the back of this data book for a list of AMD approved third party programmers.

MACHXL Software Documentation

MACHXL software is accompanied by the MACHXL software User's Manual, a concise and complete guide to MACHXL software syntax, fitting, and simulation. The manual also offers design tips on how to take advantage of MACH 3 and 4 device architectural features, and includes a few short design examples.

Updates and Maintenance

MACHXL software sold by AMD comes with one year of free maintenance updates and technical support. After the first year, maintenance can be purchased for a nominal charge.

PHYSICAL DIMENSIONS*

*For reference only. BSC is an ANSI standard for Basic Space Centering.

PL 084
84-Pin Plastic DIP (measured in inches)